Readout electronics for the wide aperture Silicon Tracking System of the BM@N experiment at NICA

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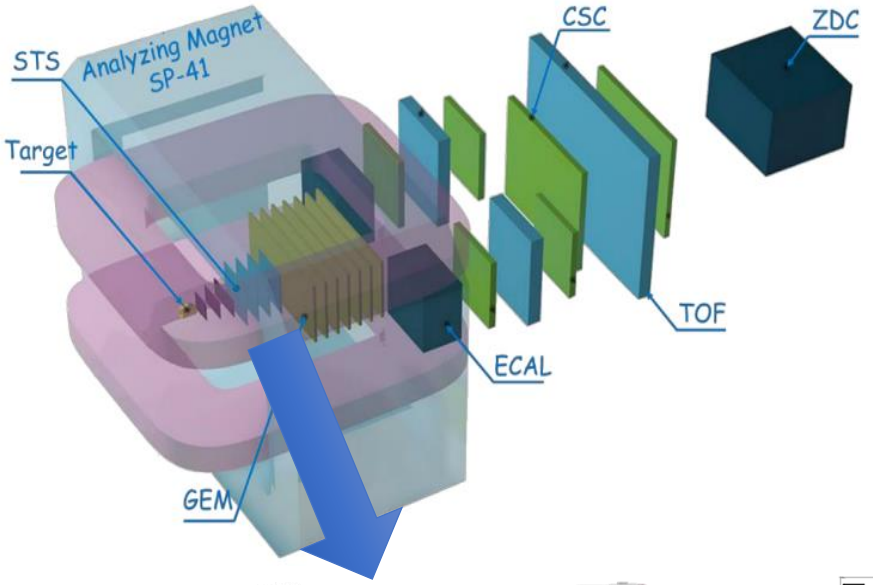
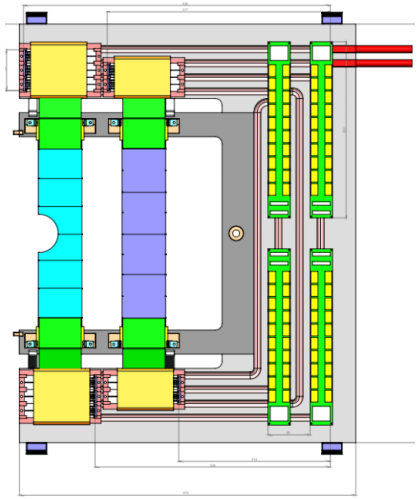
LXXII International conference "NUCLEUS – 2022. Nuclear physics and elementary particle physics. Nuclear physics technologies“
11-16 July 2022

The Silicon Tracking System (STS)

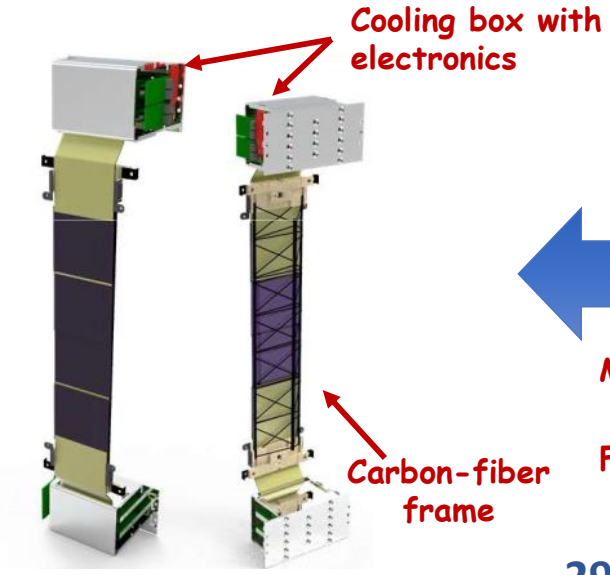


- Double-sided silicon microstrip sensors;
- Hit spatial resolution ≈ 25 μm;
- Low-mass detector modules/ladders;
- Self-triggering front-end electronics;
- Time-stamp resolution ≈ 12,5 ns;
- Total power consumption: ≈ 10 kW.
- ≈ 600k readout channels;

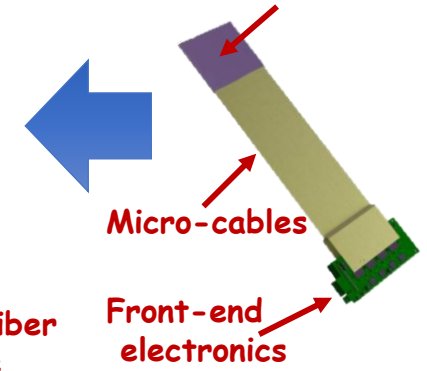
4 Stations



16 Quarter-Stations

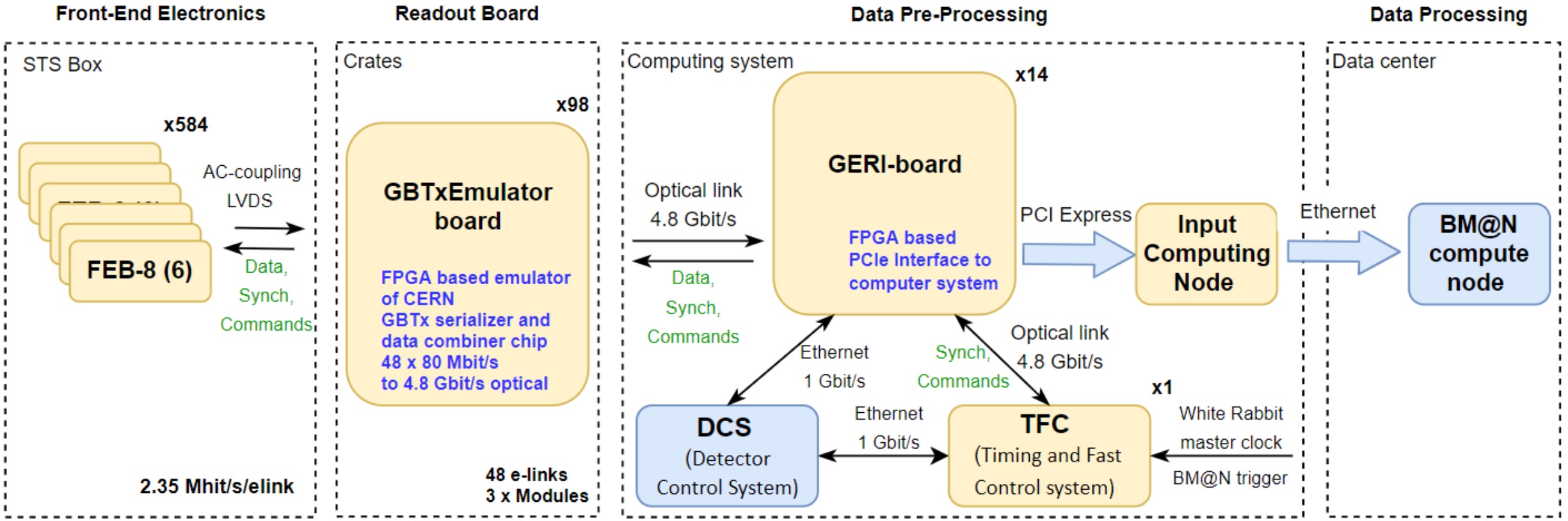


44 Ladders



292 Silicon strip modules

STS Data Acquisition (DAQ) System

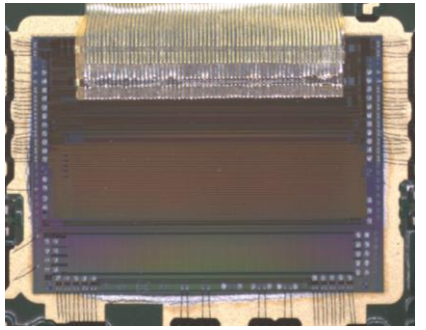


Inherits design of the CBM readout chain developed for 10 MHz HI IR

STS Module

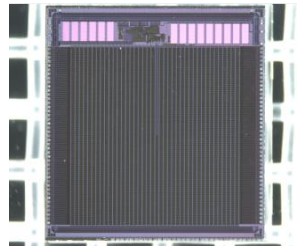
- Double-sided;
- Thickness is 300 µm;
- 1024 strips of 58 µm pitch;
- Stereo angle 7.5°;
- 2 variants/strip lengths

x8



STS-XYTER ASIC

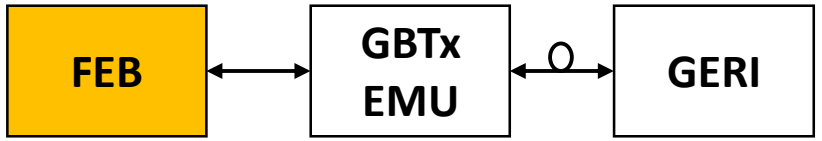
x4



Low-dropout Regulator ASIC

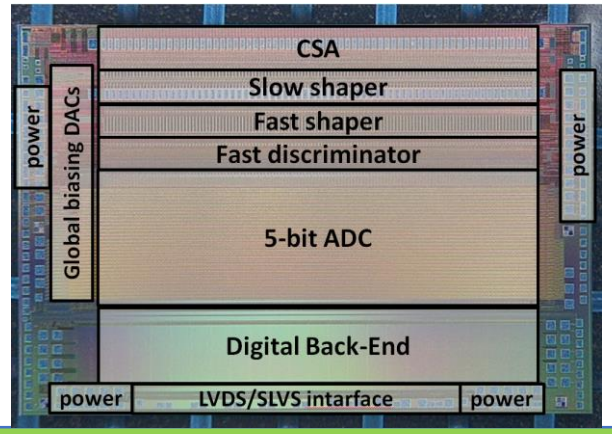
- 8 STS-Xyter ASIC per FEB;
- Size: 87*40*3 mm;
- AC-coupled LVDS links;
- The use of components of the minimum available size
- Bonding of cables with sensors;
- Wire-bonding of ASIC on the PCB;
- Energy consumption: 12 W

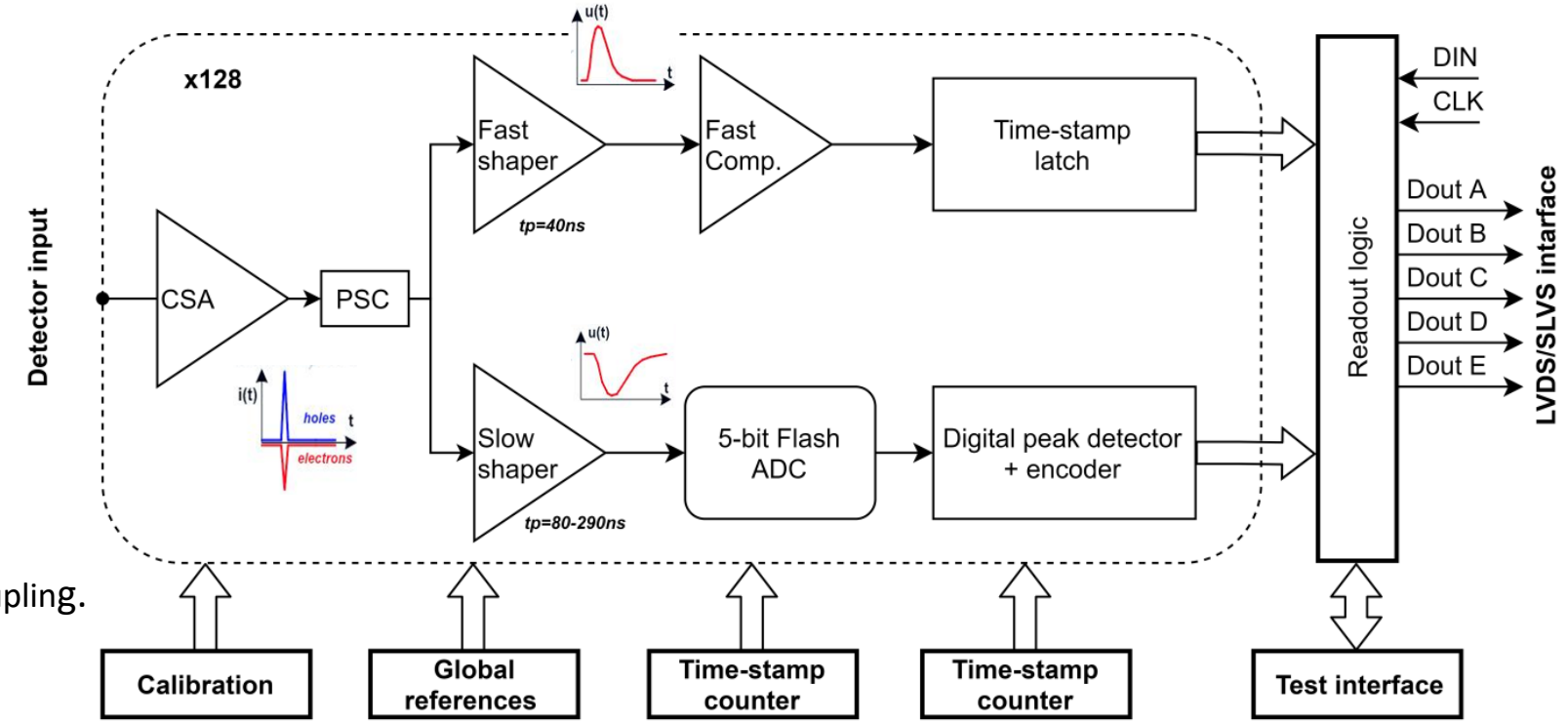
Front-end readout ASIC



Front-end electronics is based on STS-XYTER v.2.2 ASIC

- 128 channels;
- Self-triggered readout;
- UMC CMOS 180 nm process;
- Unpackaged circuit;
- Great flexibility of the analog and digital part;
- Dynamic range (up to 15 fQ);
- 5 bit ADC, time resolution < 8 ns;
- Shaping time 80-120 ns (Slow Shaper for Amp.);
- Noise performance: <1500 ENC with sensor;
- Back-end interface : 5 e-link per ASIC with AC coupling.

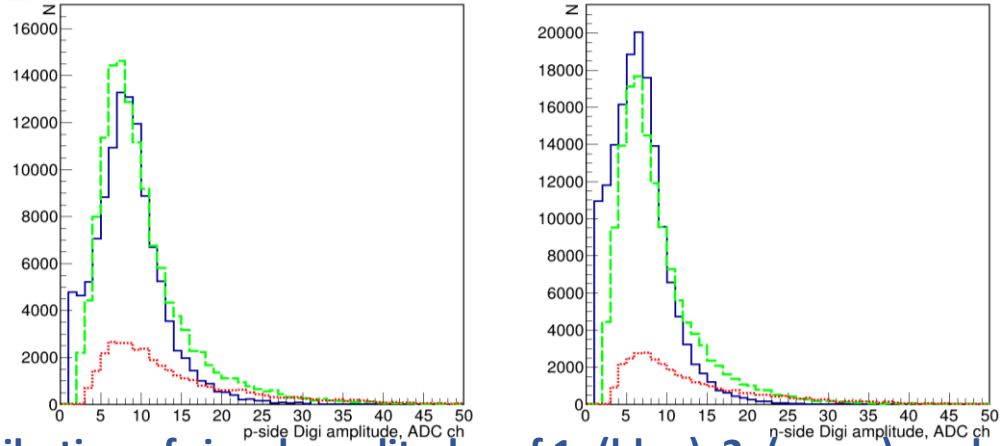




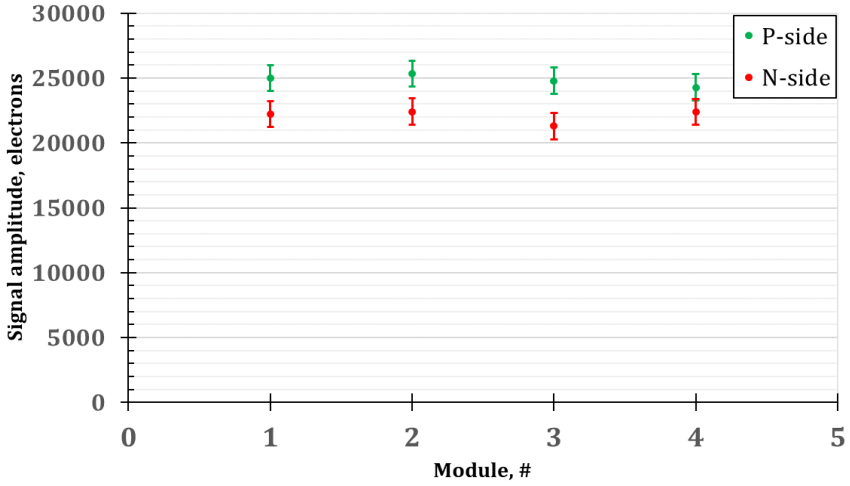
Block diagram of the architecture of the STS-XYTER

**developed by*
K.Kasinski et. all, AGH (Krakov)
for CBM collaboration

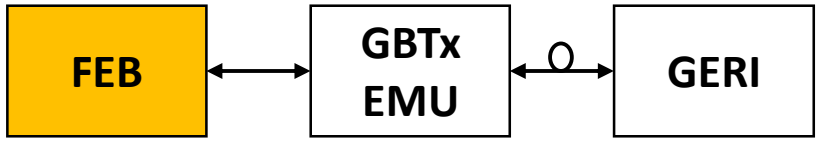
Signal-to-Noise ratio

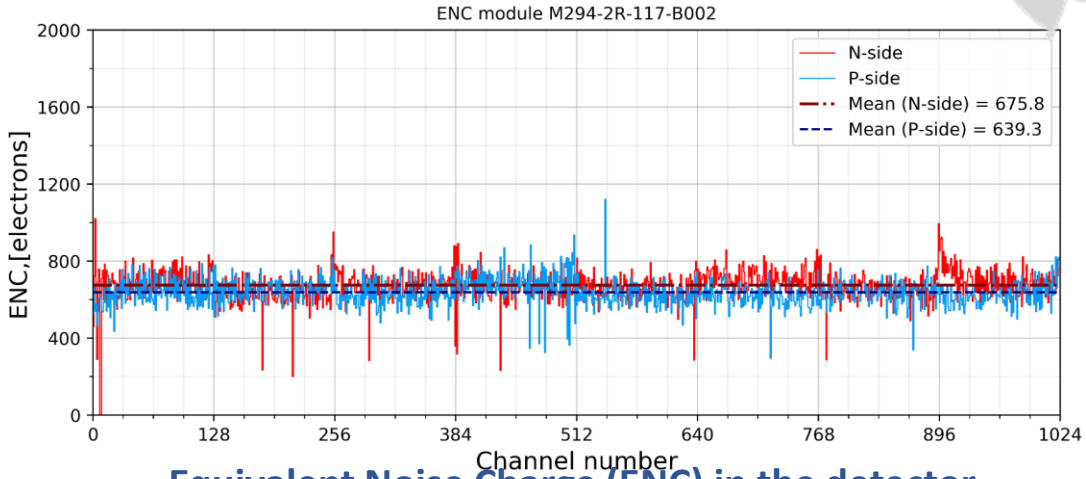


Distribution of signal amplitudes of 1- (blue), 2- (green), and 3 (red) strip clusters from beta-source Ru^{106} on the P (left) and N (right) sides of the module

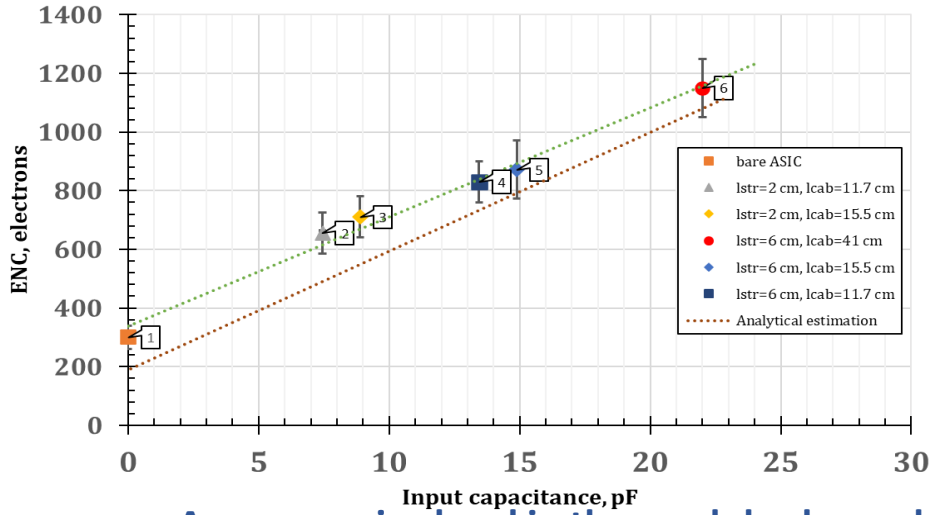


Average value of signal amplitudes from beta source Ru^{106} for 4 different modules





Equivalent Noise Charge (ENC) in the detector channels on the P- (red) and N- (blue) sides.



Average noise level in the module channels for different module configurations.

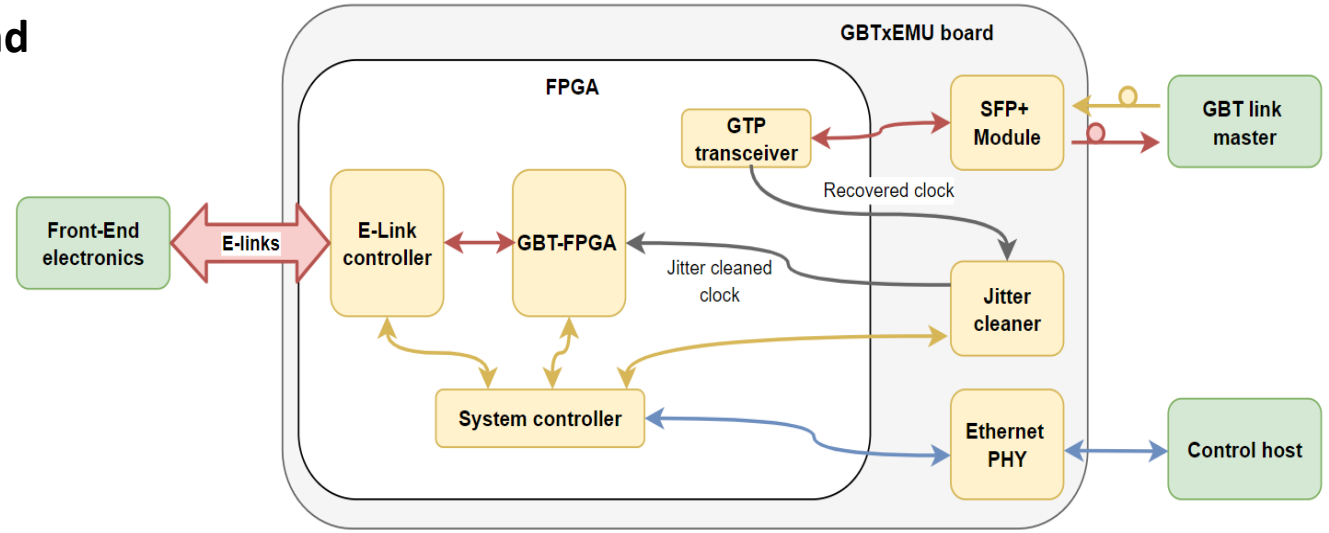
GBTxEmulator

Provide interface between the Front-End Electronics and the Data Processing board

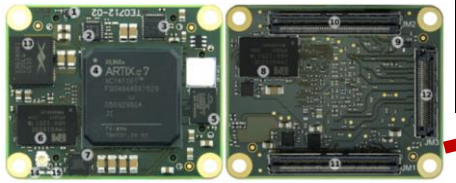
Features:

- Provides GBTx ASIC functionality;
  - Fast time deterministic transport of downlink massages;
  - high-speed transmission of hit data in the uplink direction;
- Platform: Trenz TE0712-02-100-2C from Xilinx;
- 3.75 Gb/s link optical links connecting with the GERI;
- Control interface: IPbus via 100 Mb/s Ethernet;
- E-Link interface:
  - 48 E-Links with 80 Mb/s data rate;
  - 6 clocks 40 MHz E-Link clock (80 MHz);
  - 6 downlink.

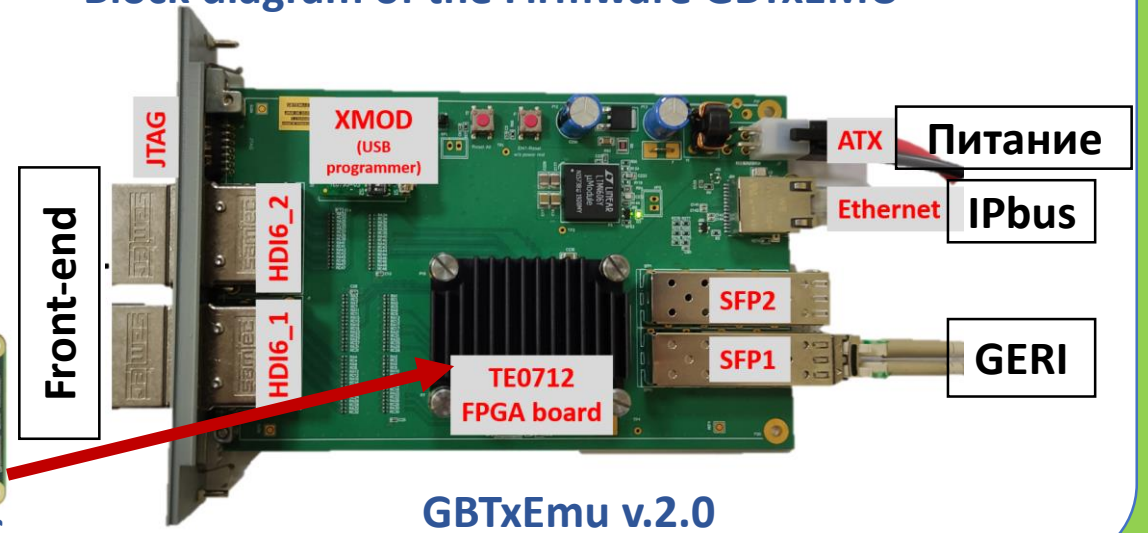
FW developments by WUT group:
W. Zabołotny at all



Block diagram of the Firmware GBTxEMU



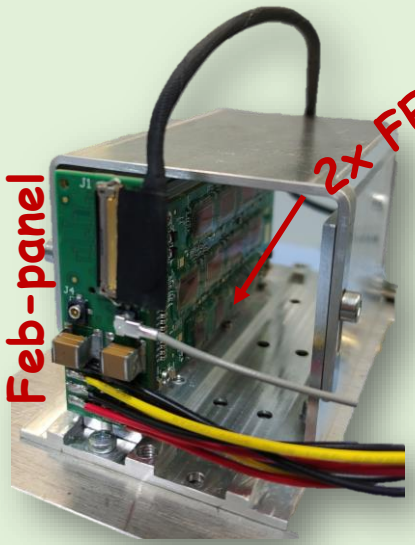
Trenz TE0712-02-100-2C



GBTxEmu v.2.0

Connectivity: FEB - GBTxEMU

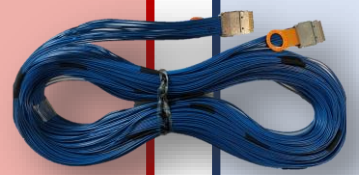
FEB ↔ GBTx EMU ↔ GERI



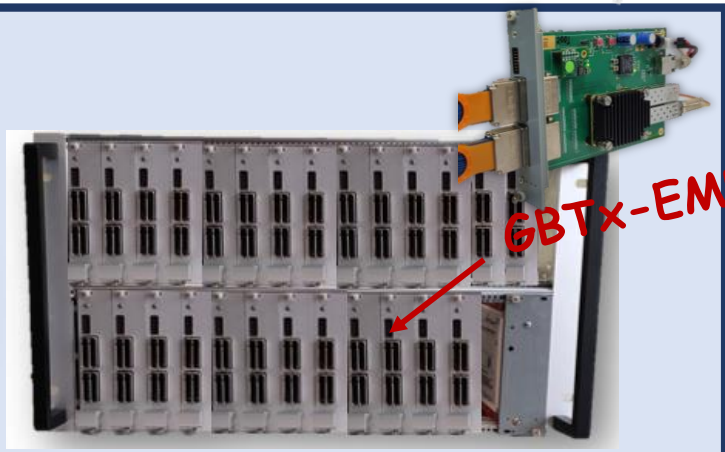
FEB-box

Microcoax. cable
≈0.7m long

Cross-panel



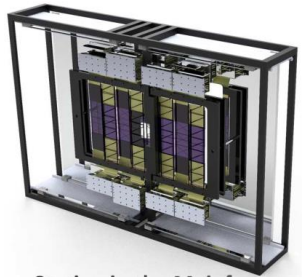
Twinax cable
10m long



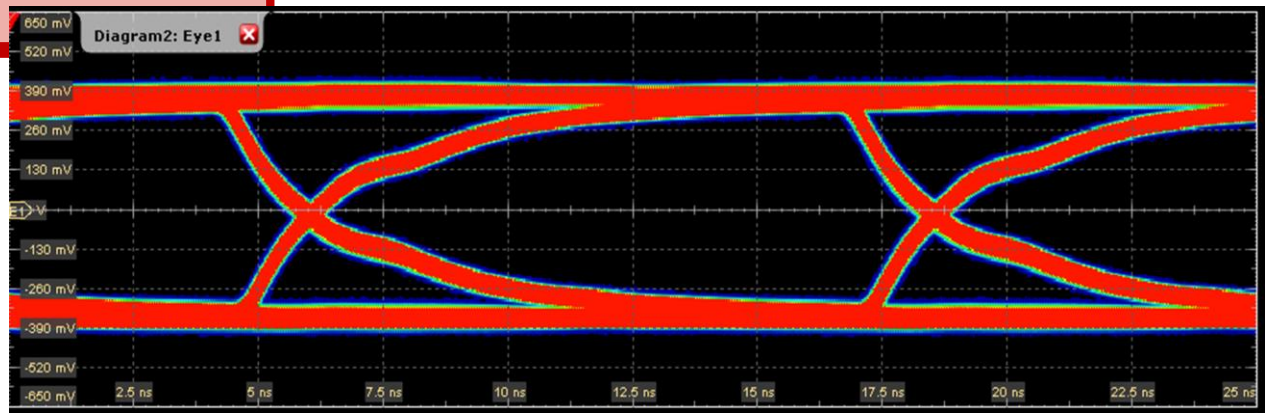
6U crate

Safe area

Inside STS station

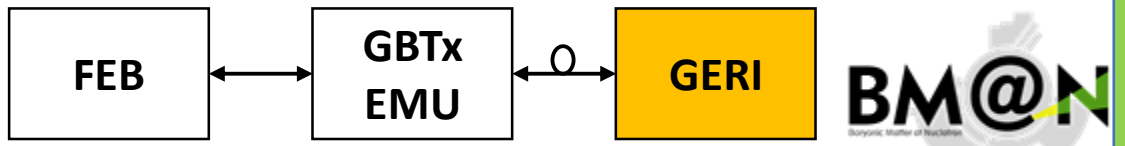


Dipole magnet



Eye diagram of the Downlink signal at 80 MHz Clk

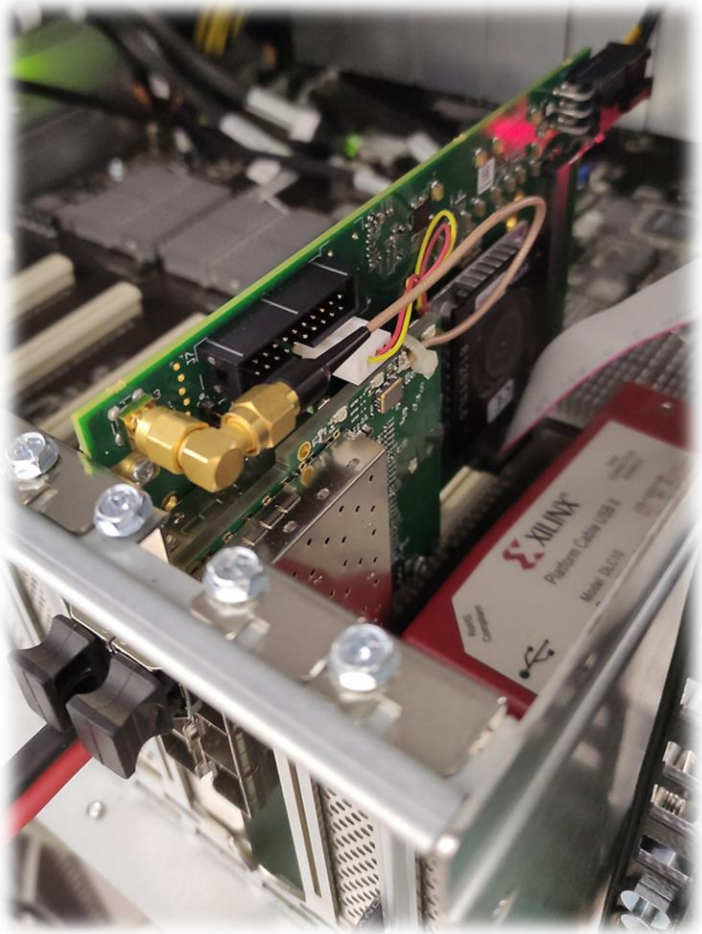
General Emulator Readout Interface (GERI)



Is based on the commercial platform: TRENZ TEC0330-4

- XILINX Virtex7 FPGA based.
- Preprocessing of the data.
- Timing and control interfaces.
- Trigger interface.
- 7 GBTxEMU boards could be connected.

TRENZ TEC0330-4 Interface Board



GERI installed in server

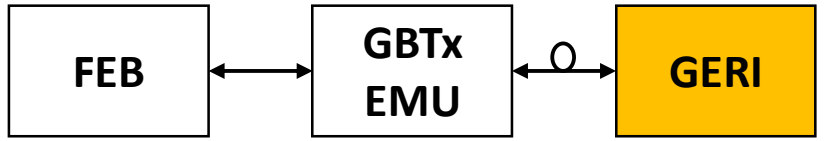
Done

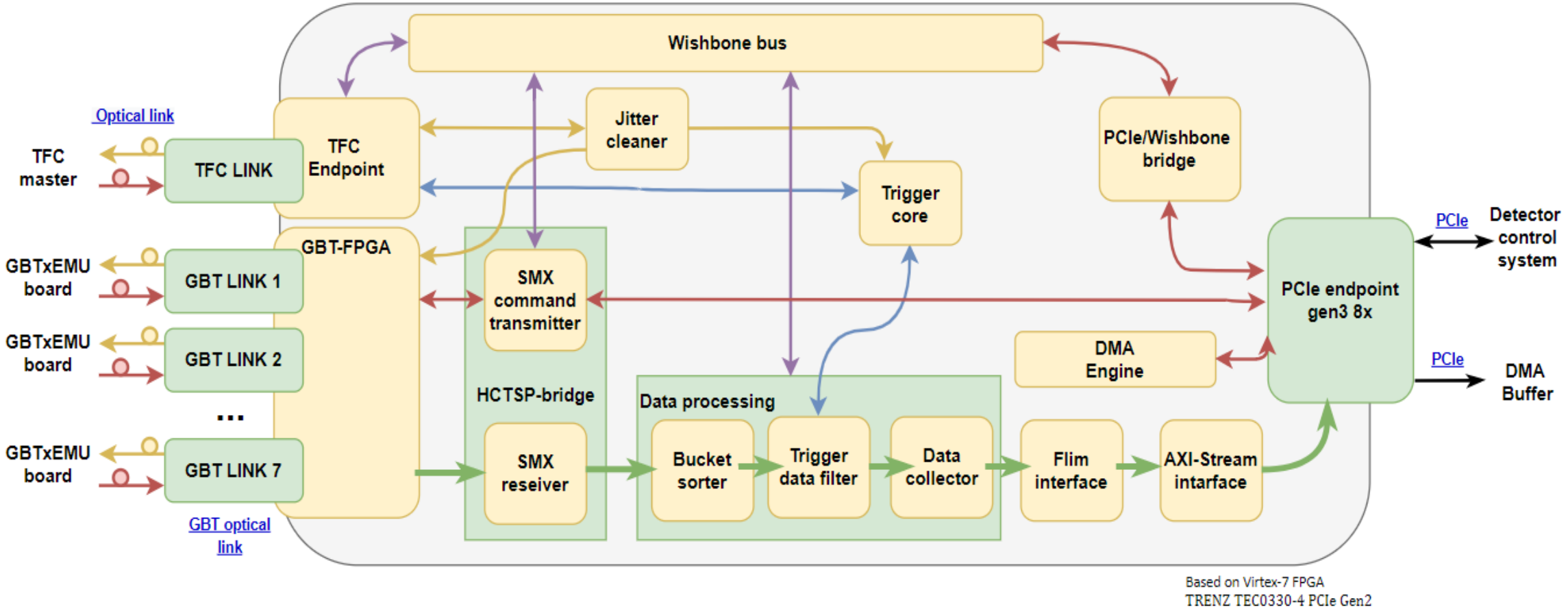
- Test setup with a GERI and remote access was installed at JINR;
- Some firmware blocks have been developed: GBT-FPGA core, PCIe core with DMA engine, DMA driver, AGWB managed Wishbone bus, trigger core;

In progress

- Integrate TFC system core;
- Combine all blocks and debug the system.

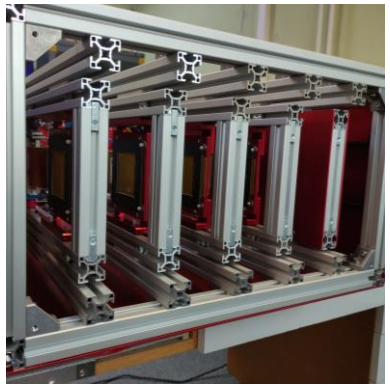
GERI firmware Block Diagram



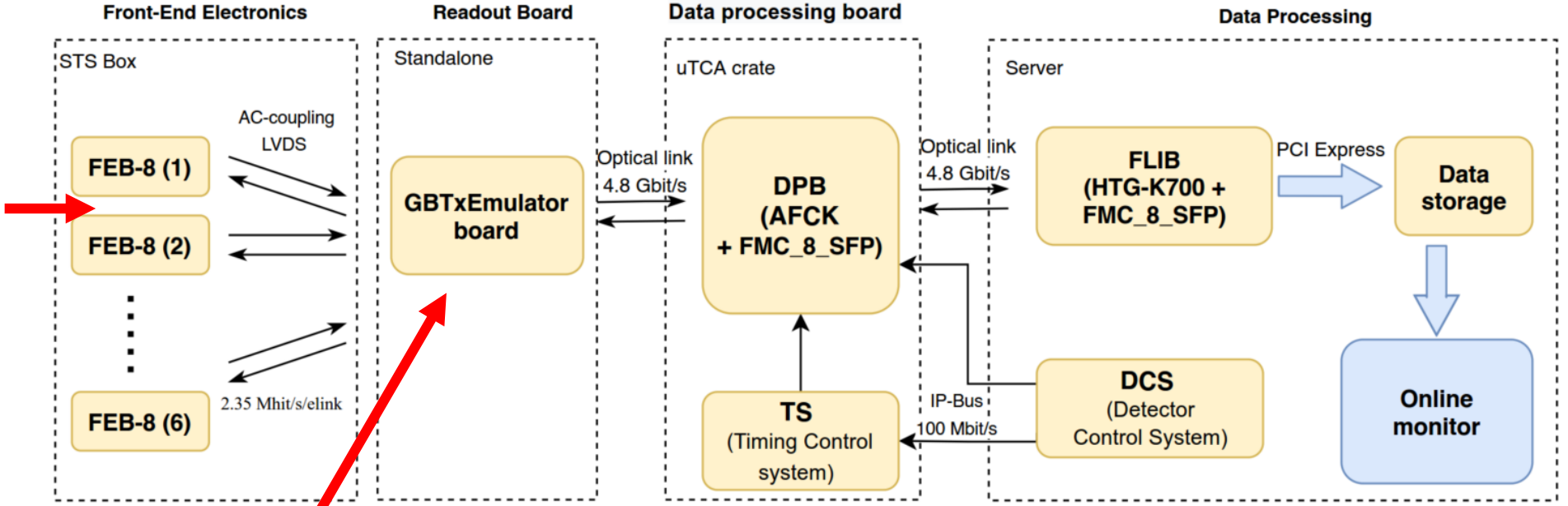


FW developments by WUT group: W. Zabołotny at all

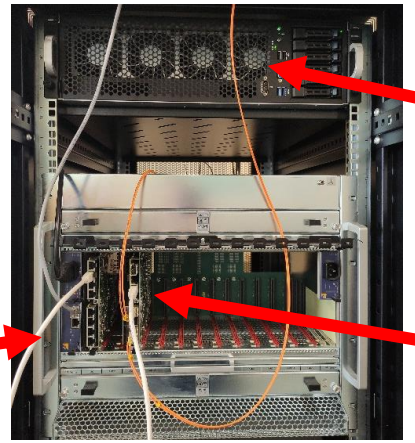
Prototype DAQ system



STS Modules



GBTxEmulator



uTCA crate

Server

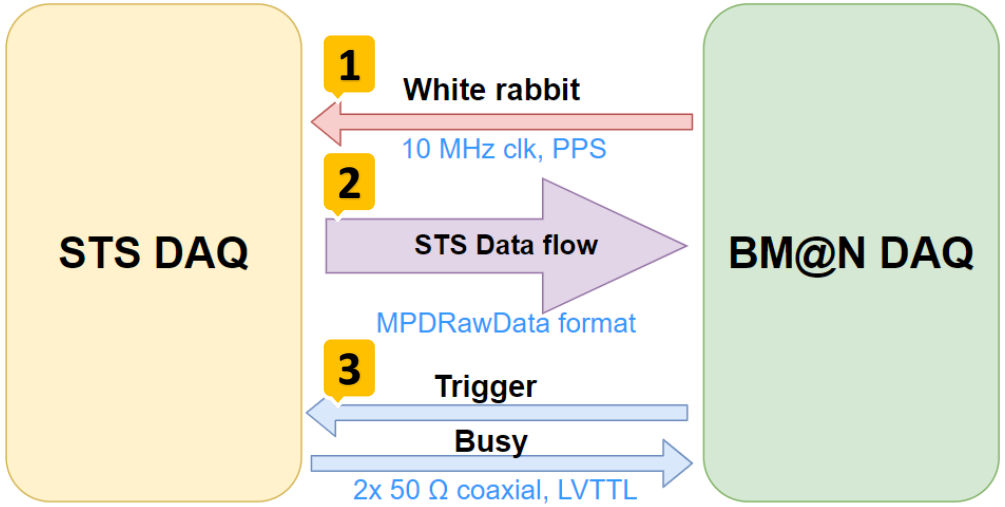
FLIB

AFCK (Data Processing Board)

Integration in the global BM@N DAQ

(1) Synchronization of the STS clock system with the WR network used in BM@N

- The concept of using 10 MHz clock and PPS signal as a reference for the STS clock domain was elaborated and tested;
- It was approved that the proposed solution allows to achieve the quality of the synchronization between STS and WR clock systems on the level <1ns;
- The first blocks of the firmware for TFC module have been developed;



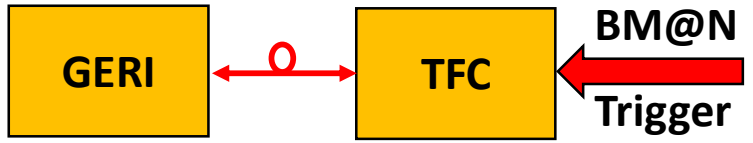
(2) Integration of the STS data stream in the BM@N DAQ

- The PCIe-based engine for high-performance data transport is prepared;
- The software application for the transmission of the incoming STS data via 1Gb Ethernet to the BM@N data processing center is being implemented;

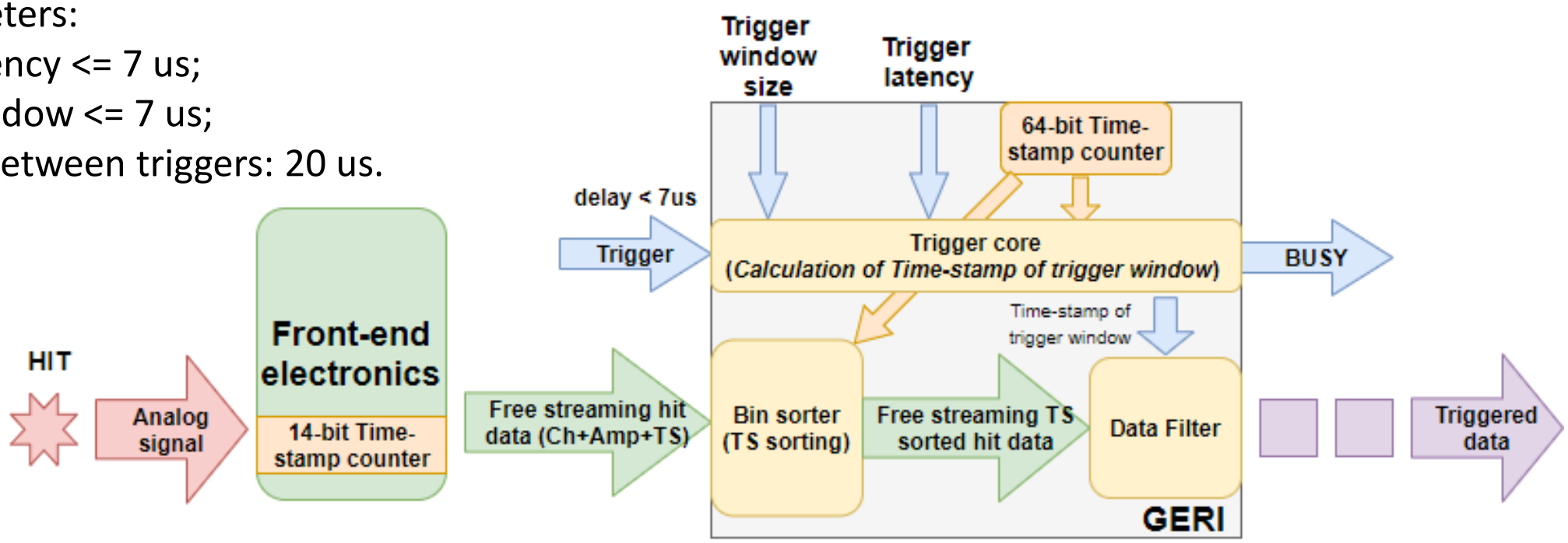
(3) Integration of the free streaming STS readout in the triggered data acquisition system of BM@N

- The concept of the triggered data acquisition is elaborated and implemented;
- Triggered acquisition was tested on the laser test bench with a full STS-module readout chain;

Trigger implementation



- The front-end electronics of STS operates only in the self-triggered mode.
- The data filtering according the trigger decision is implemented in the GERI.
- Due to the free-streaming readout scheme, GERI provides the functionality of the time-based data sorting.
- The sorters store the data for the sufficient amount of time (up to 96 μs) and thus provides the possibility to implement also trigger-based data filter.
- The concept of the triggered acquisition is elaborated and implemented.
- Trigger parameters:
  - Trigger latency <= 7 us;
  - Trigger window <= 7 us;
  - Min time between triggers: 20 us.



The results of testing of the readout chain

Done:

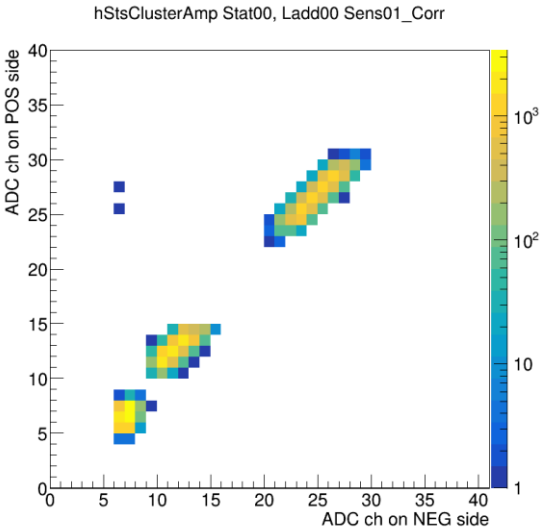
- ❑ Developed test bench for certification of assembled modules
- ❑ Tests with a laser setup were performed
- ❑ Laboratory tests of modules with radioactive sources were performed

Plans:

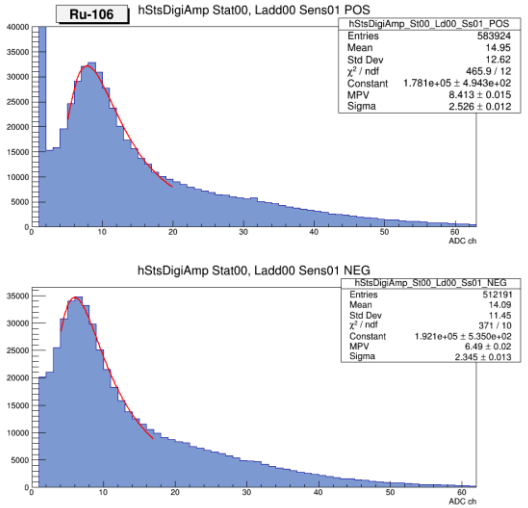
- ❑ In-beam tests of STS module based telescope at NRC «Kurchatov Institute» (PNPI) in Gatchina
- ❑ Irradiation tests of GBTxEmu
- ❑ In-beam tests of STS ladder at PNPI

Performance:

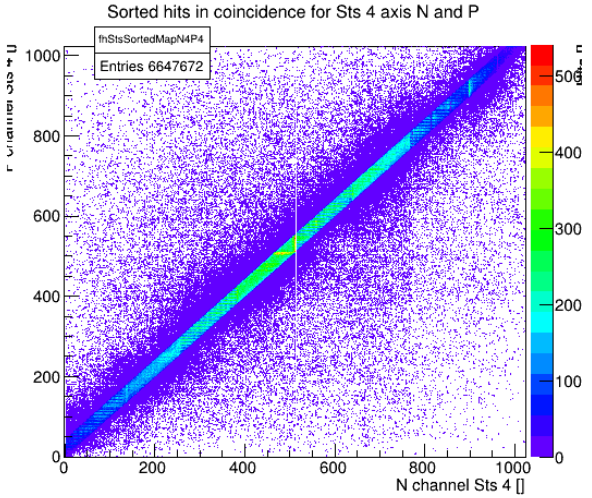
- noise: ~800 e- (N-side); ~700 e- (P-side);
- r/o threshold: ~5000 e-;
- signal-to-noise: > 20;
- hit detection eff.: > 95%;



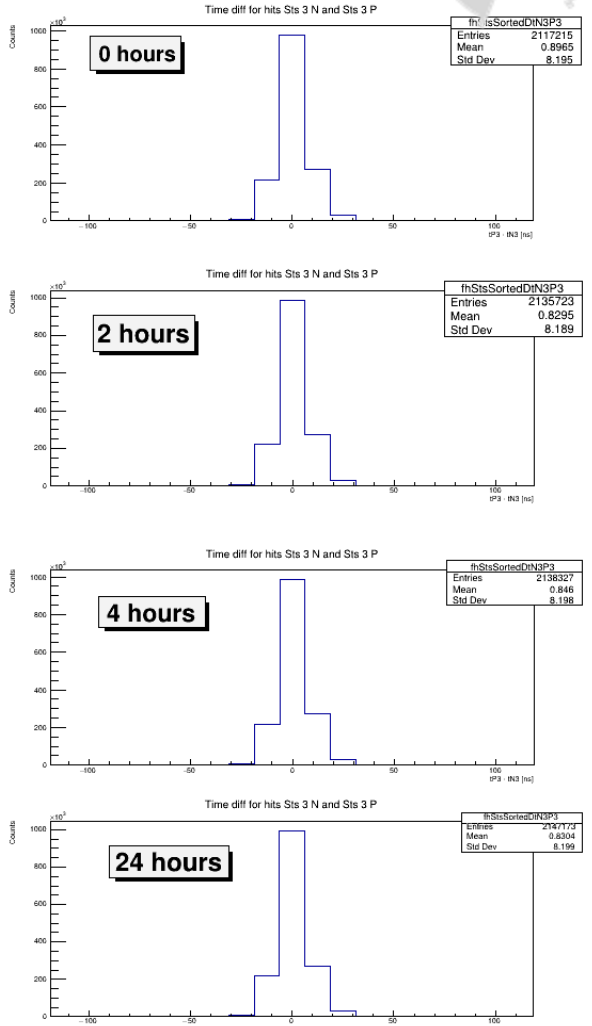
Signals from IR laser pulses (diff. amplitudes) On P- and N- sides



Signals on N- and P- sides (Ru-106 source)



Correlations between N- and P- sides



Long term stability test: quality of the time synchronization between ASICs on the P- and N- sides of the module

Summary

- BM@N STS readout chain was elaborated and is being implemented.
- GBTxEmulator was designed as a replacement for the GBTx ASIC
- Developed and implemented the concept of integrating the streaming data acquisition system of BM@N STS with the global BM@N DAQ.


Thank you
for your attention!