Test of full PSD readout chain at the mCBM

F. Guber, D. Finogeev, N. Karpushkin, A. Makhnev, S. Morozov, D. Serebryakov

Institute for Nuclear Research RAS, Moscow, Russia;

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Outline

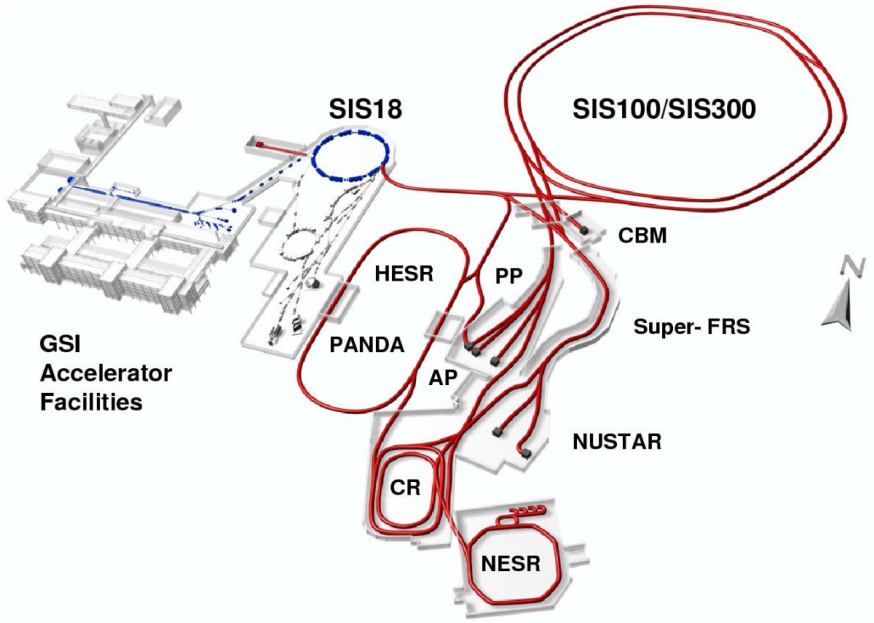
- CBM experiment at FAIR
- Projectile Spectator Detector (PSD) at the CBM experiment
- Readout system of the PSD calorimeter
- Results of mPSD beam tests at mCBM
- Conclusions

CBM @ FAIR – Facility for Antiproton and Ion Research

Based on GSI (Helmholtz Centre for Heavy Ion Research), Darmstadt, Germany:

- ➢ Primary beams (SIS100):
- Heavy ions (up to $^{238}U^{92+}$) - 11 GeV/u, 10^{10}/s
- Protons - 30 GeV, $3x10^{13}$/s

- ➢ Secondary beams:
- Ions - 1.5 - 2 GeV/u
- Antiprotons - 1.5 - 15 GeV



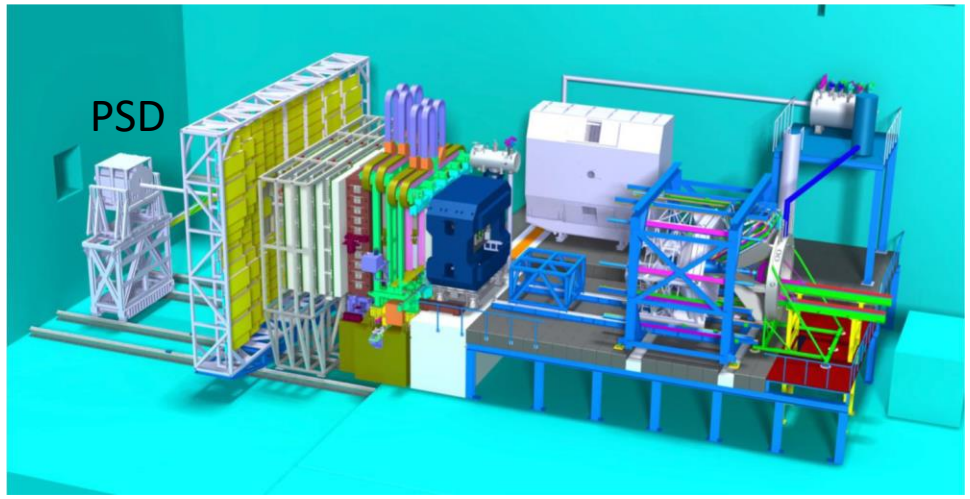
FAIR includes 4 large experiments:

- Atomic, Plasma Physics and Applications - **APPA**
- Compressed Baryonic Matter - **CBM**
- Nuclear Structure, Astrophysics and Reactions - **NUSTAR**
- antiProton ANnihilation at DArmstadt - **PANDA**

- FAIR is an international accelerator facility under construction
- Commissioning is planned for 2025.

Compressed Baryonic Matter (CBM) experiment

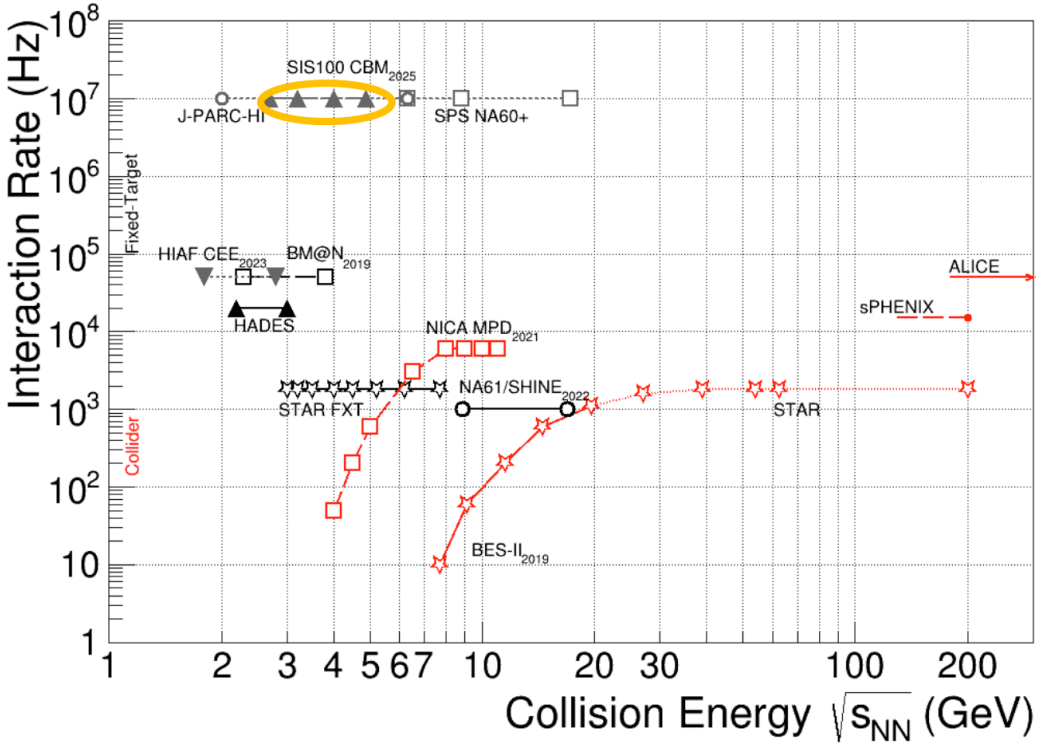
The primary goal of the physics program of the CBM is the exploration of the QCD phase diagram in the region of high baryon densities.



Physics program will be focused on measurements:

- Short-lived light vector mesons decaying into lepton pairs
- strange baryons containing more than one strange quark;
- mesons containing charmed quarks;
- collective flows of all observed particles and their fluctuations.

- Heavy-ion beams: Au + Au at 4 to 11 AGeV; beam intensity: 10^9 ions/sec; reaction rate 10 MHz
- First-Day experiment: $5x10^7$ ions/sec; reaction rate – 0,5 MHz



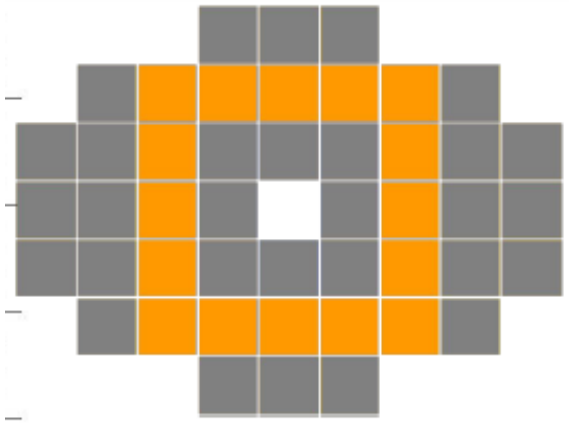
Main experiment requirements:

- Identification of charged hadrons and leptons
- Measurement with high accuracy of momentum of secondary particles
- Definition of interaction vertex (σ ~ 50μm)
- Determination of reaction plane and centrality

Requirements for FEE and DAQ system:

- Radiation tolerant Front-End Electronics
- Trigger-less, high rate readout system
- Online event reconstruction and event selection

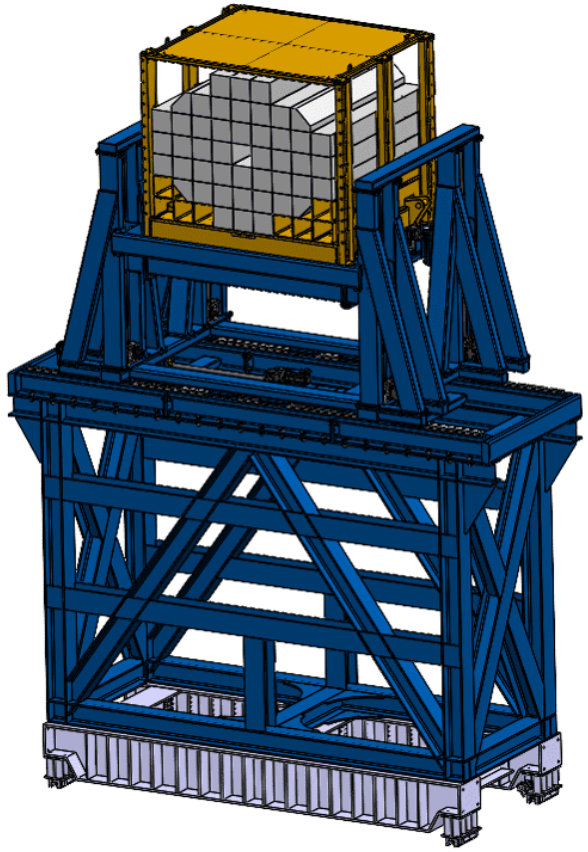
Projectile Spectator Detector (PSD)



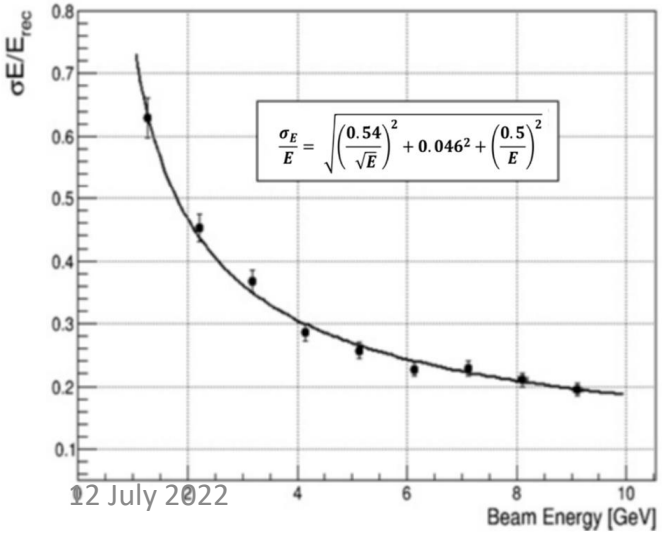
PSD configuration for Day-1 CBM experiment

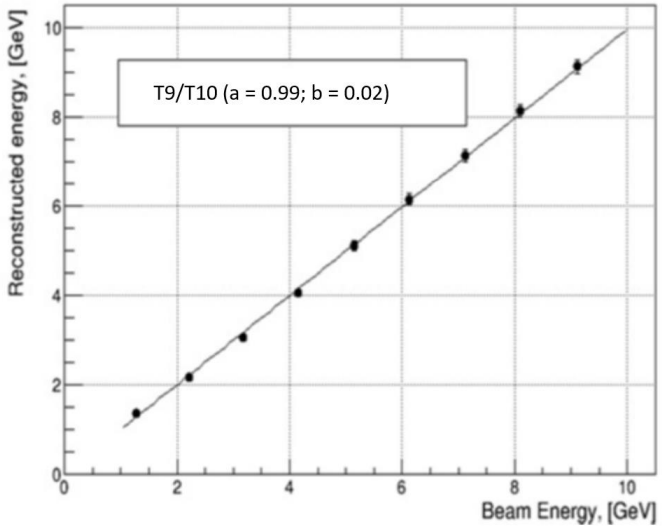
The main purpose of the PSD is the measurement of centrality and orientation of reaction plane in heavy ion collisions at interaction rate up to 10^6 per sec.

- PSD - sampling lead/scintillator forward hadron calorimeter with beam hole in the center.
- PSD – modular structure: 46 modules 20x20x165 cm^3.
- Total weight – 23 tons.
- PSD will be placed at distance ~10.5 from the the target.

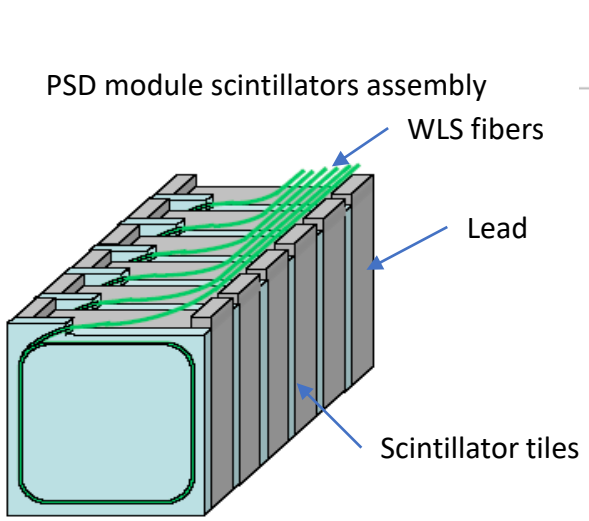


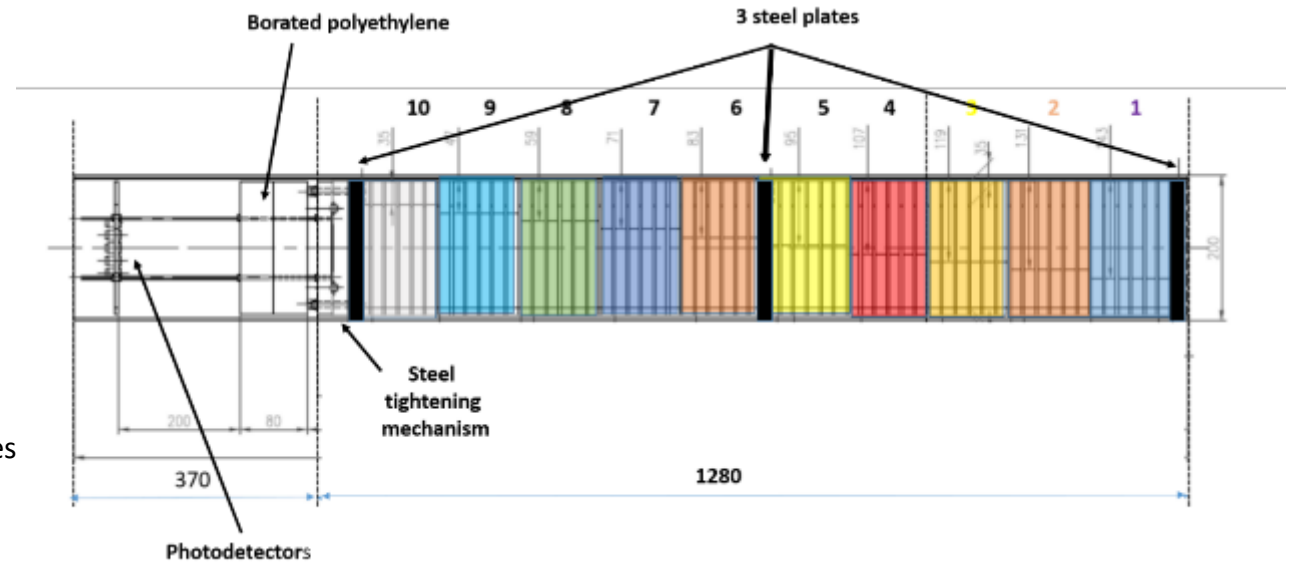
Energy resolution and linearity response (T9/T10 testbeam at CERN)





Structure of the PSD modules





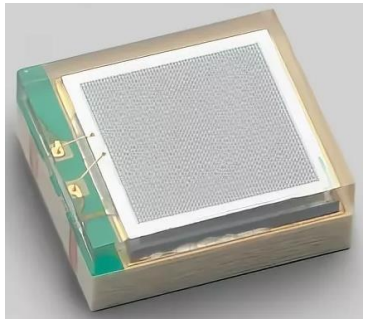
PSD module - 60 Pb/scint. samples. (Pb (16mm) + Scint (4mm))

- Length of the module – 5.6 λint
- Light collections – 6 WLS fibers from 6 sequentially scint. tiles combined into one optical connector at the end of module.
- Light readout: 10 MPPC (3x3 mm2) per module

- Module size 20x20x165 см3.
- Weight of the PSD module – 500 kg.

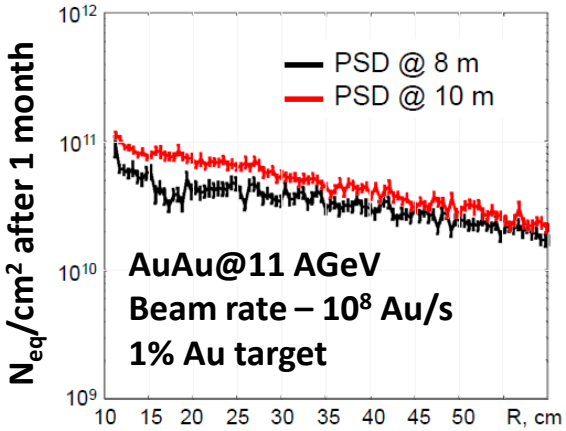
Most of cosmic and beam tests have been done with Hamamatsu S12572-010

- Sensitive area - 3 x 3 mm2
- Number of pixels - 90 000
- nominal gain - 1 x 105,
- Gain ~1% /1°C
- Pixel recovery time - 10 ns
- PDE -18%

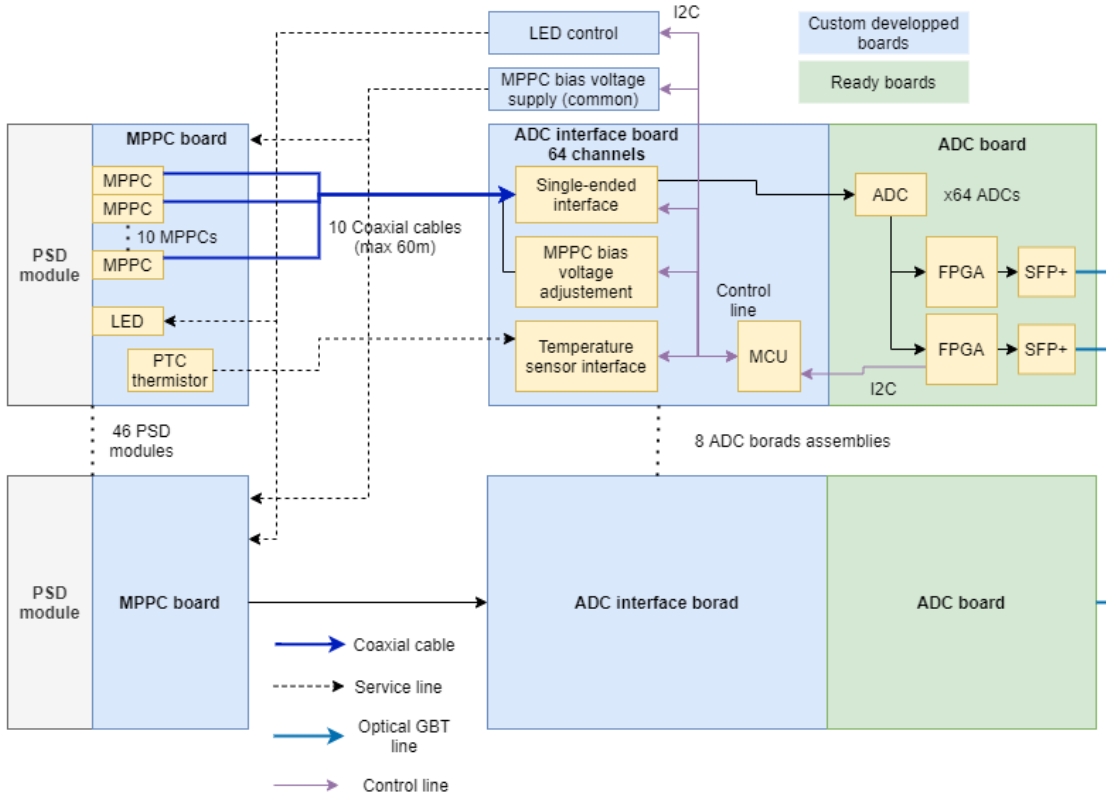


PSD Front-End readout electronics

Board with 10 MPPCs, a temperature sensor and LED for calibration are mounted on rare side of modules

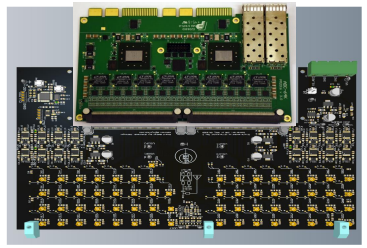


Radiation estimation at the photodetectors plate

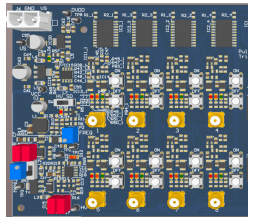


Radiation sensitive electronic will be placed in radiation safe area
Analog signals will be transmitted via 60 m coaxial cable

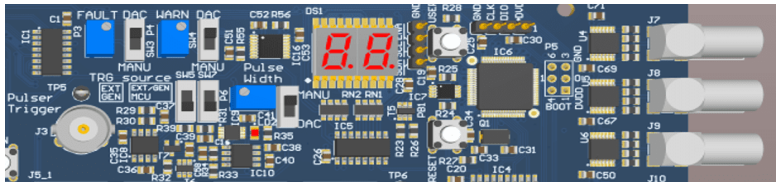
ADC board: 2xKintex 7 FPGA, 64 channels, I2C bus



MPPC bias voltage supply board



LED pulses generator board

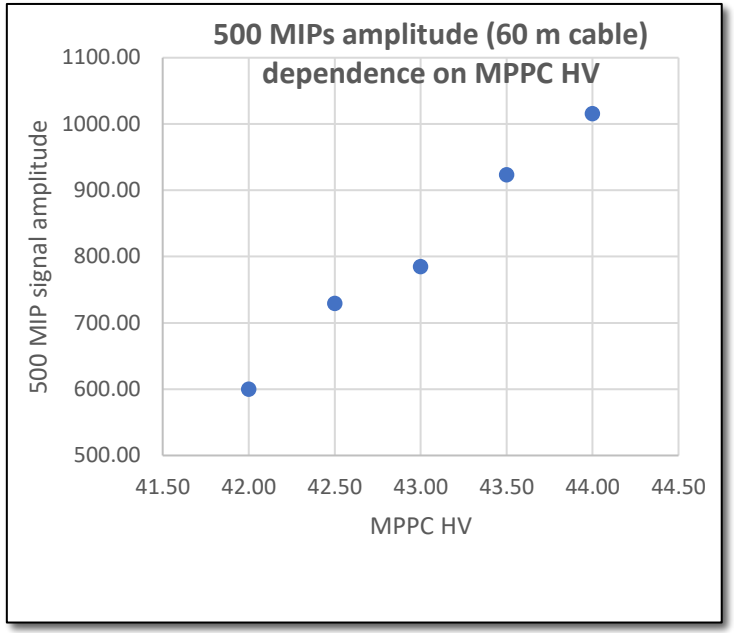


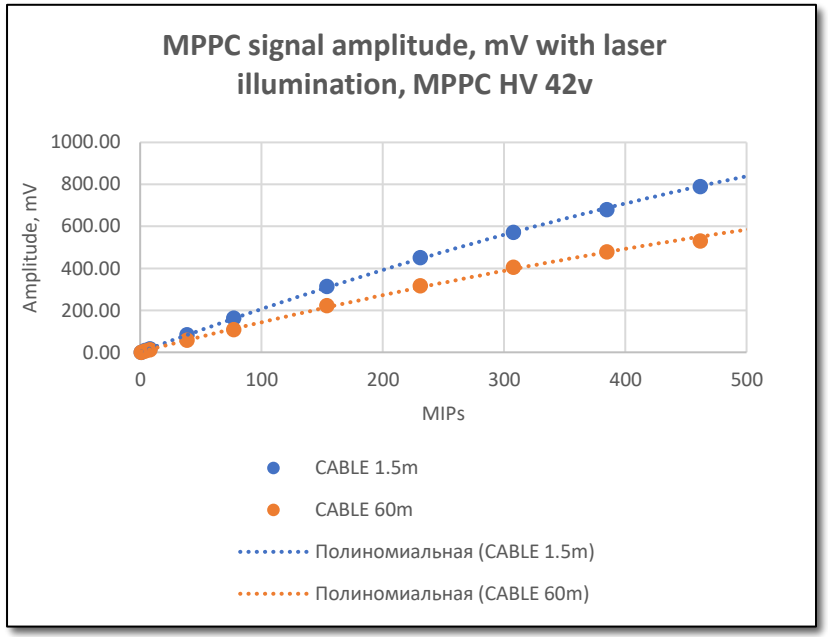
Coaxial cables 60m

Измерение динамического диапазона системы

- MPPC type S14160-010P
- MPPC response is linear in 500 MIP range
- For 60 m cable attenuation is 1.5
- Gain 2x allow to distinguish 1 MIP/pedestal

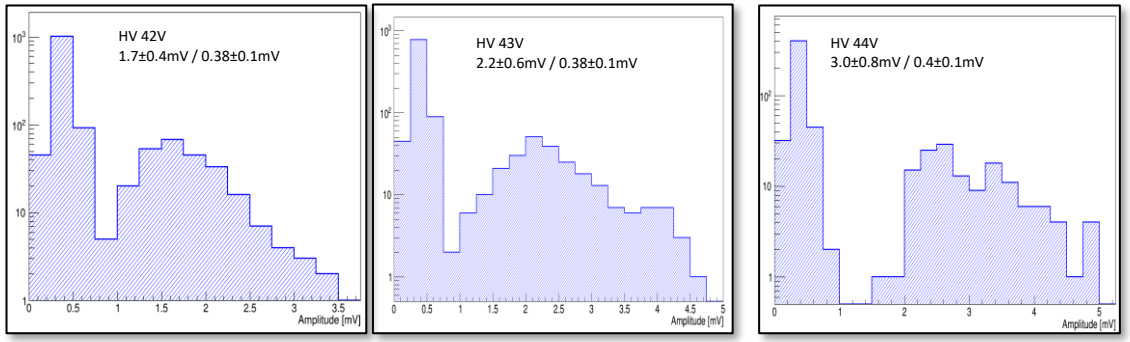
- MPPC HV operation range is 42 – 44 V
- 500 MIP pulse signal for 60m cable0 is:
  - 600mV – MPPC HV 42 V
  - 1015mV – MPPC HV 44 V

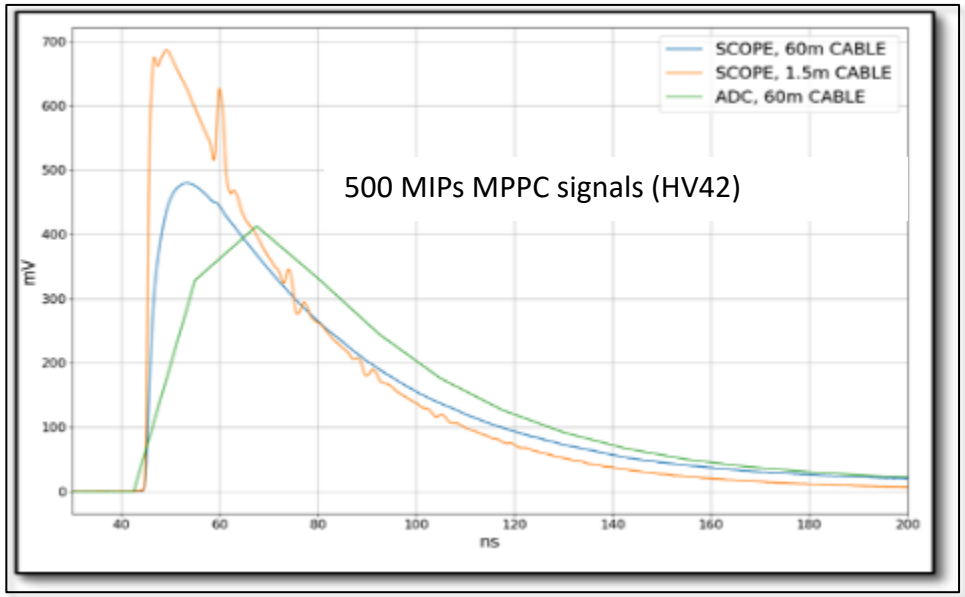




- ADC range is 2V
- To keep 500 MIP range ADC interface gain should be 2X for 44 V
- Possibility to distinguish 1 MIP is required for PSD calibration

Cosmic 1MIP peak (60m cable, gain 2X)

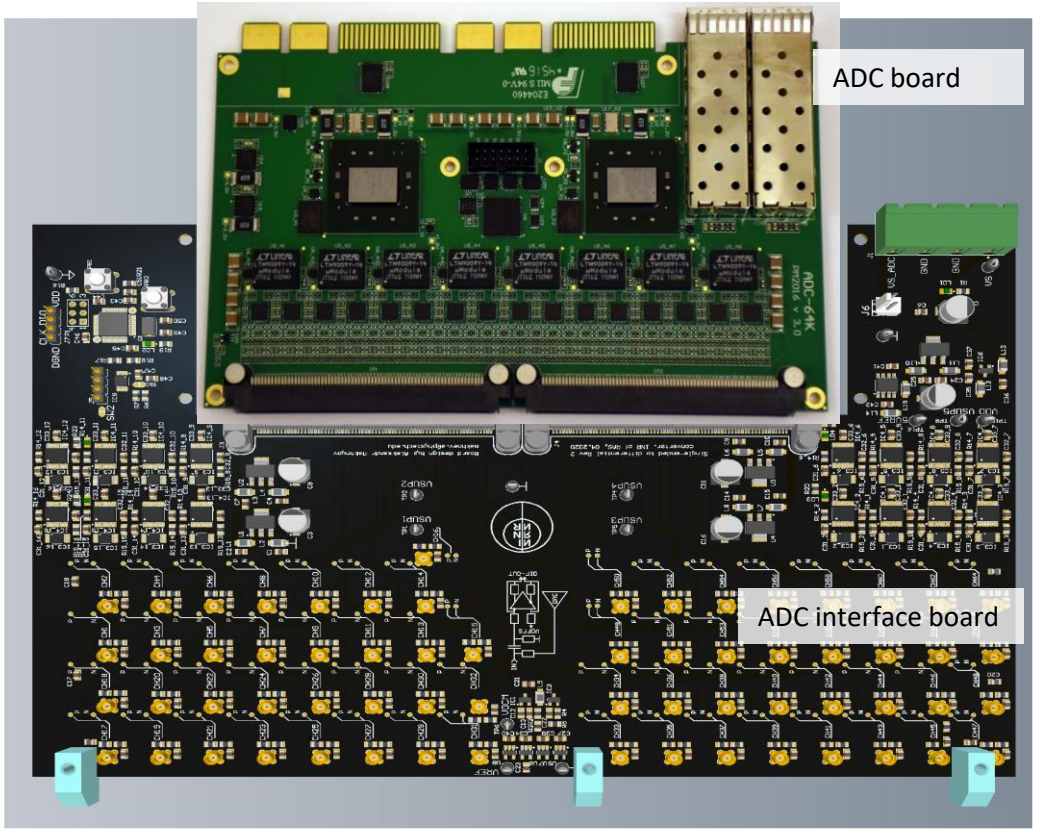




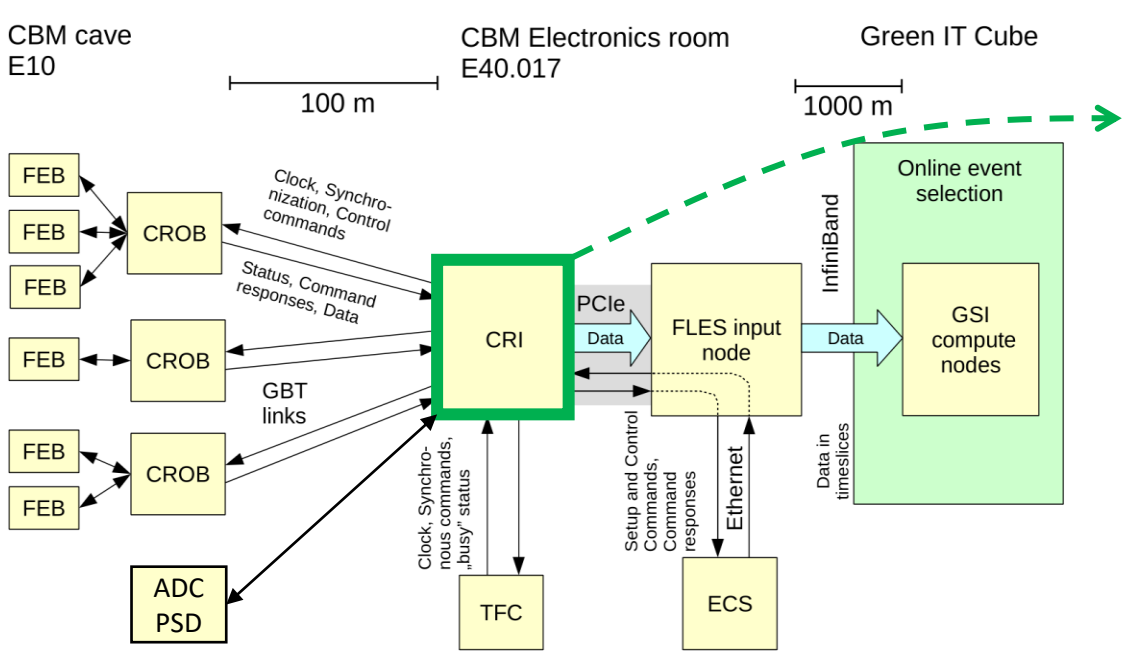
ADC board + interface board

- Two board assembly
  - **ECAL@PANDA ADC64 board**
  - LTM9011 ADC 125Msps / 80Msps (14-bit digitization; 2VP-P)
  - Two FPGA Kintex 7
    - 32 channels per one FPGA
    - Separated optical link for each

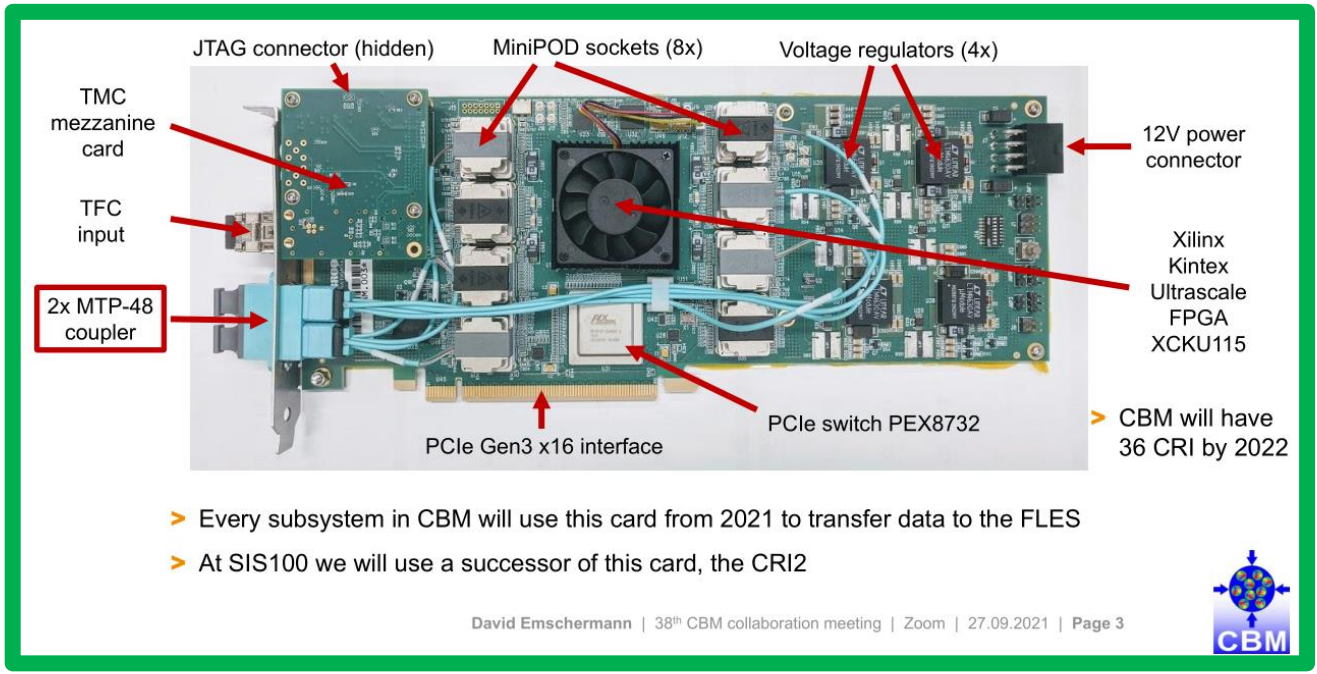
  - **Interface board designed in INR RAS**
    - ADC interface (single-ended to differential converter)
      - Adjustable input and output zero levels
      - 40 MHz bandwidth
      - 4V dynamic range
    - MPPC bias voltage individual channel adjustment circuit
    - Temperature sensor interface
    - I2C control from the ADC board



Система сбора данных эксперимента CBM



Common Readout Interface board (CRI)



CBM readout is based on CRI board

- Xilinx Kintex UltraScale XCKU115 FPGA
- 48 optical link
- Throughput PCIe gen3 x16 до 100 GB/s
- Collect and sort detector data, send data to Event reconstruction cluster

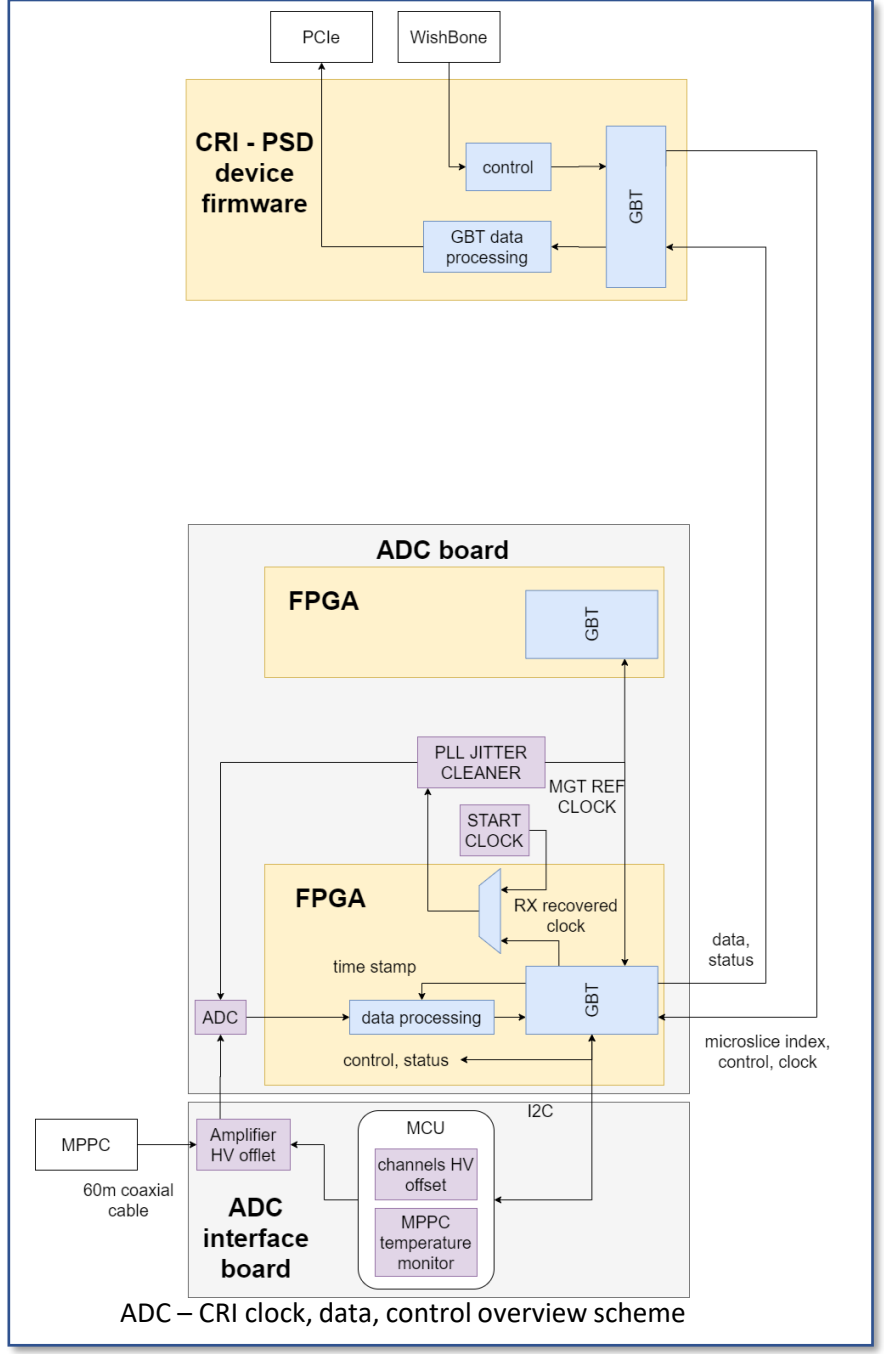
PSD readout integration into mCBM DAQ

- GBT FPGA is used for the connection to CRI board
- CRI clock is used for the ADC board
  - LMK0460 jitter cleaner is used
  - Internal clock used to synchronize GBT
  - After GBT starts provide recovered clock from CRI, the clock MUX switched GBT Rx clock
  - Time stamp provided by CRI via GBT

- The ADC boards assembly is controlled via GBT
  - The ADC FPGA is connected via I2C to MCU on the ADC interface board

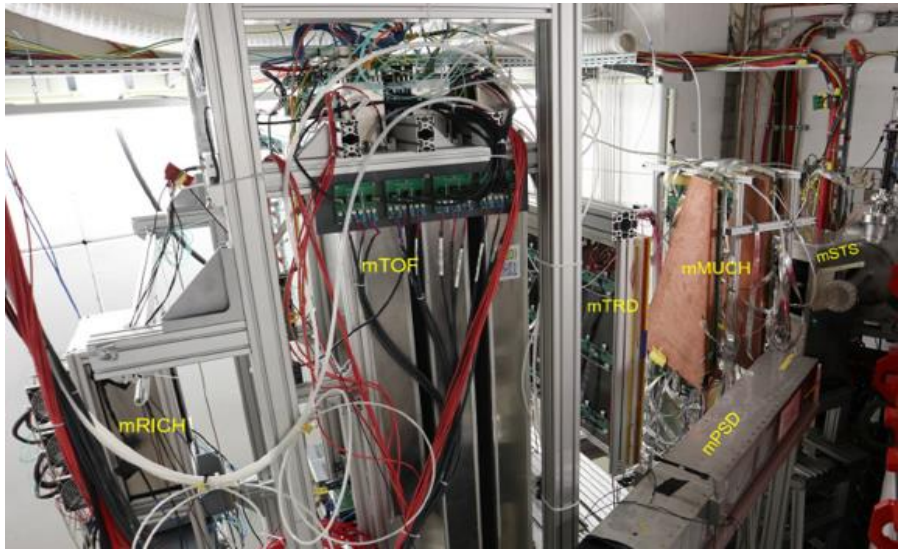
- Current FPGA design allow to digitize data at 1 MHz hit rate per channel

Results are published in:
"The readout system of the CBM Projectile Spectator Detector at FAIR"
DOI: 10.1088/1748-0221/15/09/C09015



ADC – CRI clock, data, control overview scheme

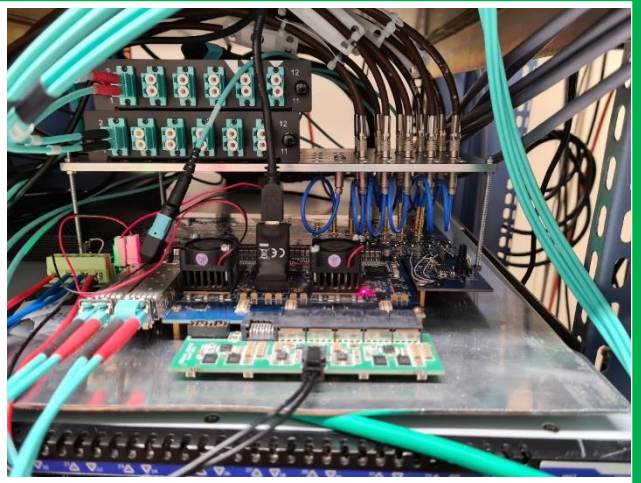
mPSD @ mCBM



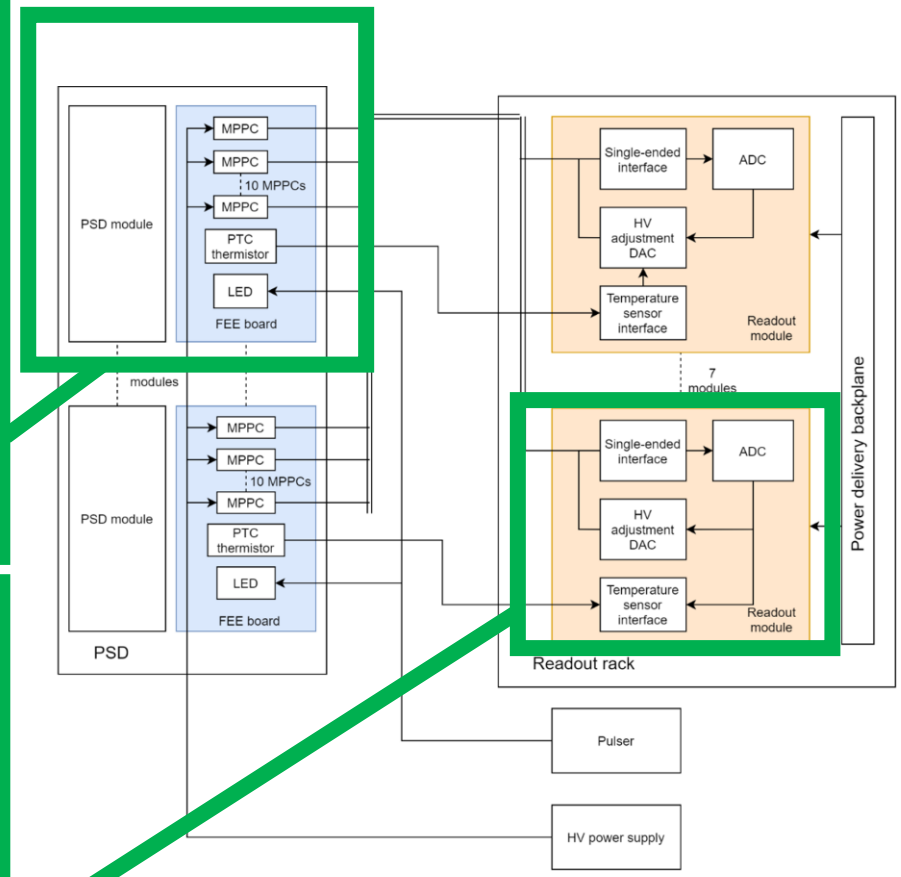
mCBM@GSI – testbeam for CBM experiment with all detectors prototypes installed with CBM DAQ prototype

- mPSD – single PSD module was installed at mCBM and integrated to mCBM DAQ
- mPSD is a full chain prototype and include:
  - MPPC board
  - ADC + interface boards assembly
  - Connection with 60m coaxial cables

MPPC board mounted on PSD module @mCBM

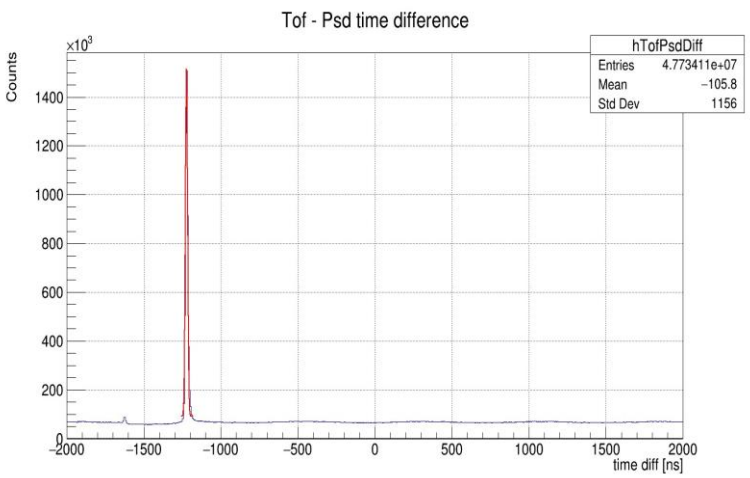


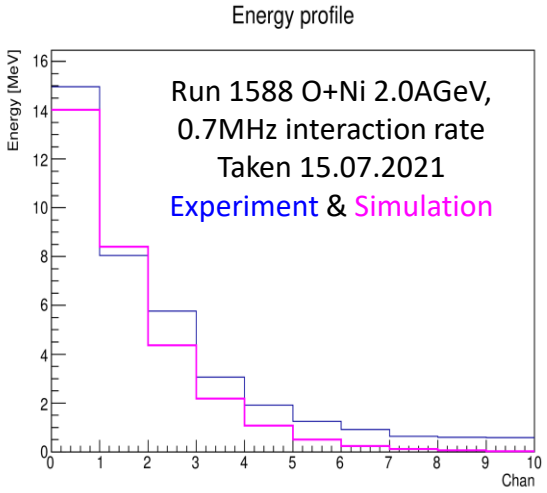
ADC64 FPGA board + interface board installed in DAQ container and connected with 60m coaxial cable to PSD module @mCBM



ADC baseline drift during high rate

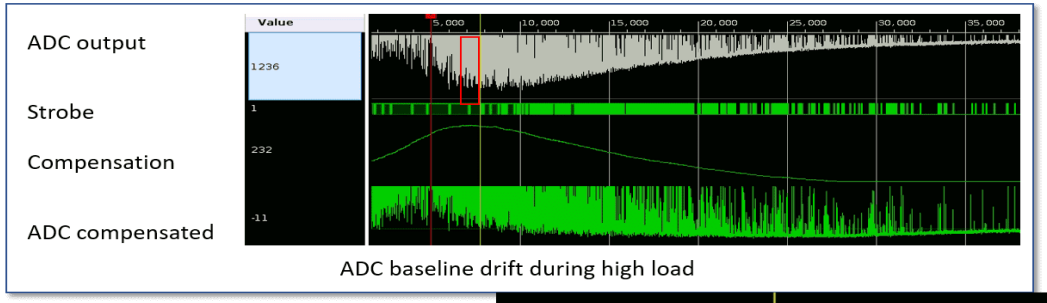
- Full chain of mPSD readout has been successfully integrated:
  - in mCBM readout and tested at high interaction rate.
  - Time correlation with other subsystems
  - mPSD energy spectra are in agreement with simulated mPSD data





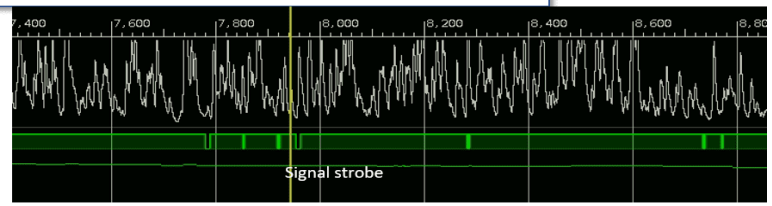
ADC baseline drift during high rate because of capacitance in FEE input filter

- The firmware exponential filter compensation was prepared for beam tests.
- Correction allowed to measure signal charge with base line drift during the beam test.
- Because of tuned threshold ~ 0.8 MIP (1,4mV) compensation accuracy was not enough to avoid continuous triggering during base line drift.
- Data processing will be based on FIR filter (Finite Impulse Response) F(i) = A(i)*c1+A(i-1)*c2+...+A(i-10)*c11



ADC baseline drift during high load

- FIR filter will allow:
  - Measure charge of overlapped signals. 10% pile-up at 1 MHz event rate
  - Event triggering without of baseline
  - Reduce the hit data size up to 20bits (4 MHz readout rate)
  - FIR filter was simulated in python with data from mCBM testbeam



Continuously signals triggering

Details in topic “Study of the mPSD response in O+Ni collisions at 2 AGeV at the mCBM”
Nikolay Karpushkin
https://events.sinp.msu.ru/event/8/contributions/425/

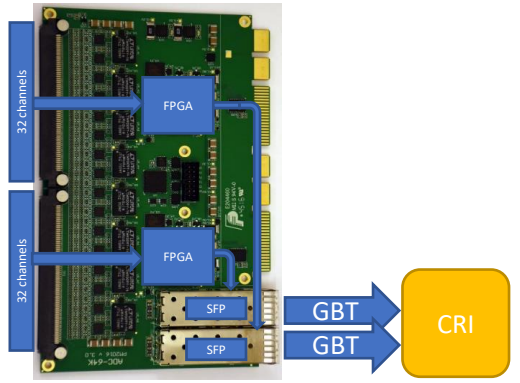
Prospects for the use of the developed readout system

- ADC clock frequency increased to 120/125 MHz
- Working on IPbus firmware integration for connection to PC

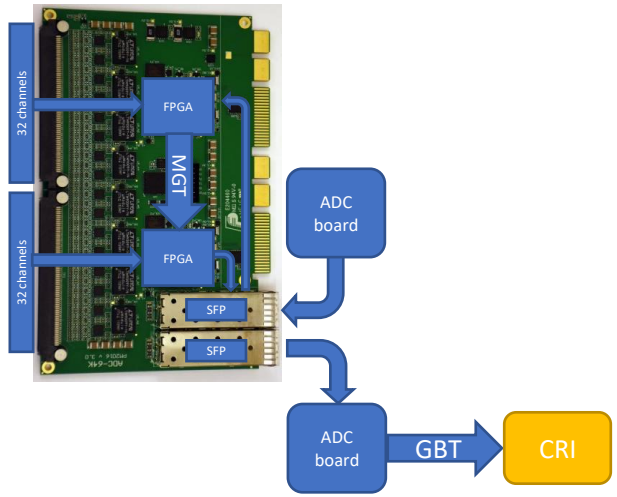
Key features:
- Radiation-hard front-end distanced 60 m to readout electronics
- Digitization rate 120 MHz (8 ns)
- Dynamic range x1200 (2.5mV – 3V, cable 60m)
- amplitude

Developed firmware for Xilinx Kintex7 FPGA could be used at custom developed ADC boards.

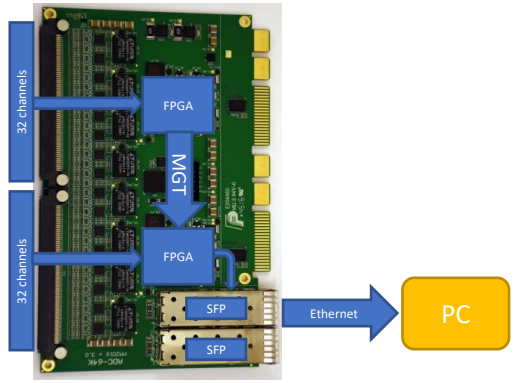
Individual FPGA connection
- High readout rate



Chain ADC board connection
- Low number of links



ADC connection directly to PC via UDP protocol (IPbus)

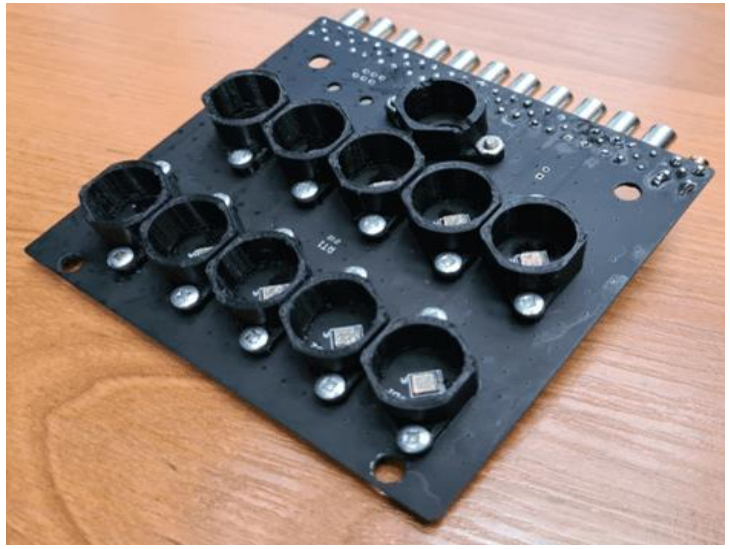


Thank you for your attention

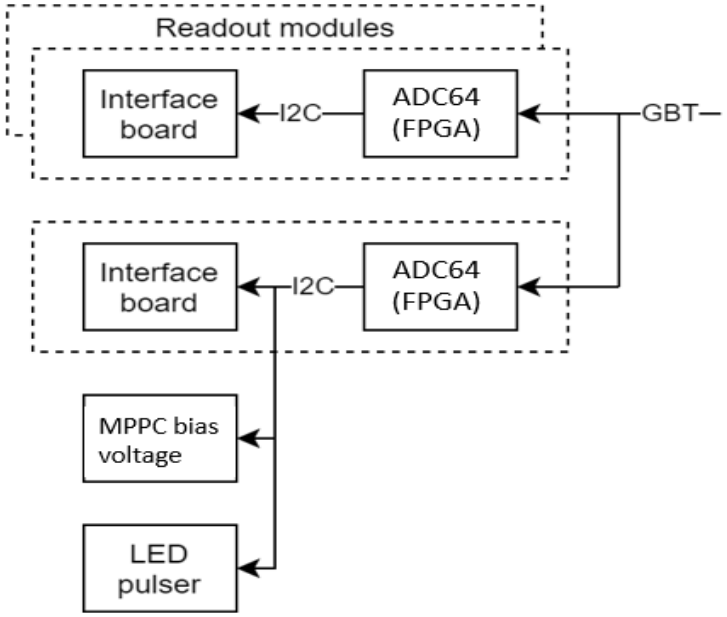
BACKUP

PSD FEE service components

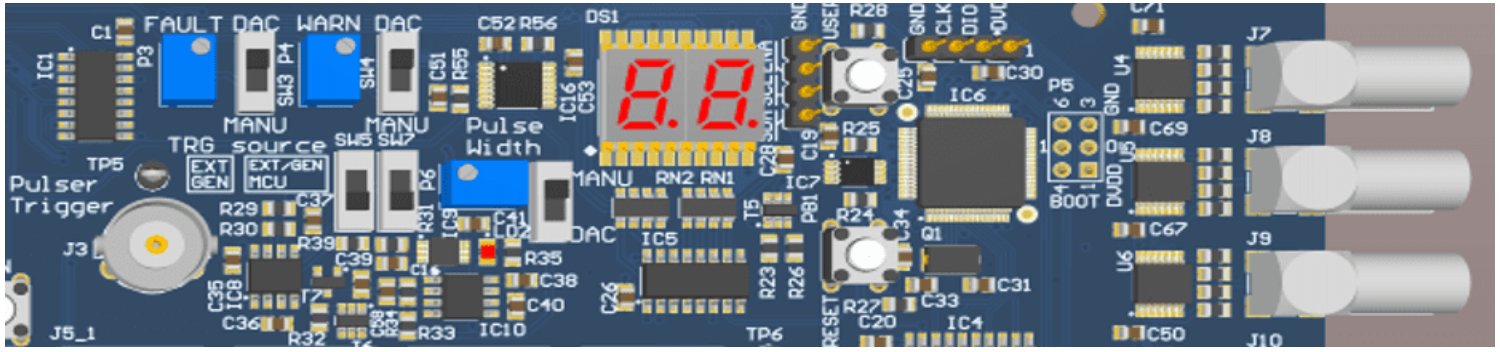
- Most crucial (MPPCs, GBT control) was tested with beam at mCBM 2021



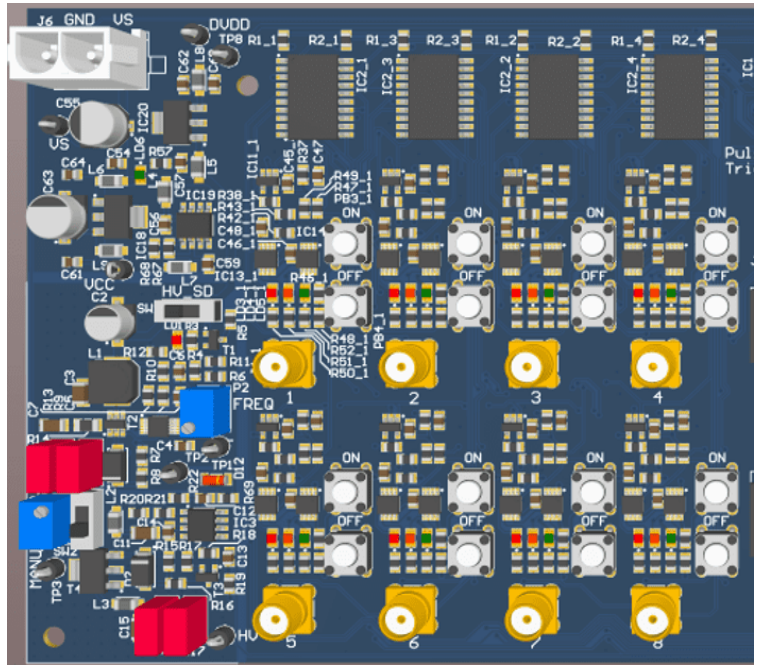
Board with 10 MPPCs, a temperature sensor and a calibration LED for each module



All PSD FEE is controlled and monitored via single point : GBT link

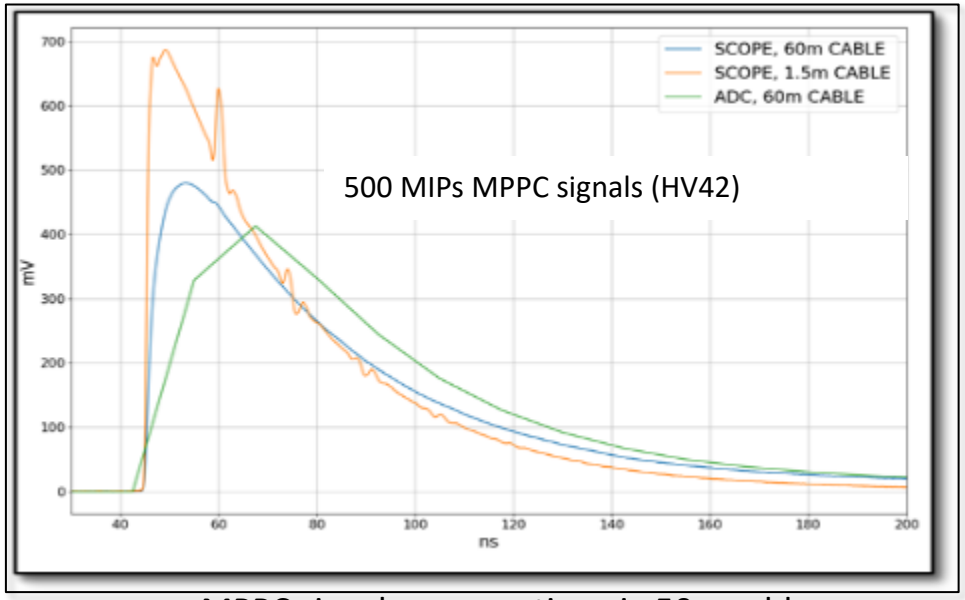


Pulse-time-stable logic pulse generator with remote control allow to fire LED for PSD calibration with external trigger or asynchronously

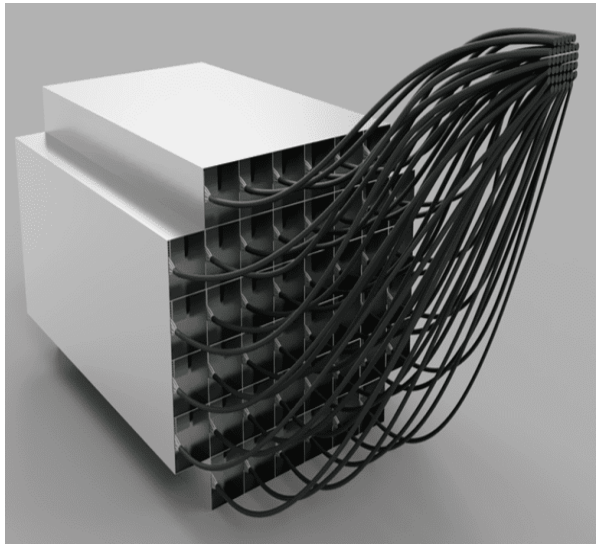


Remotely controlled MPPC bias voltage supply for MPPC biasing has been developed. Per-channel current monitoring overcurrent and short-circuit detection

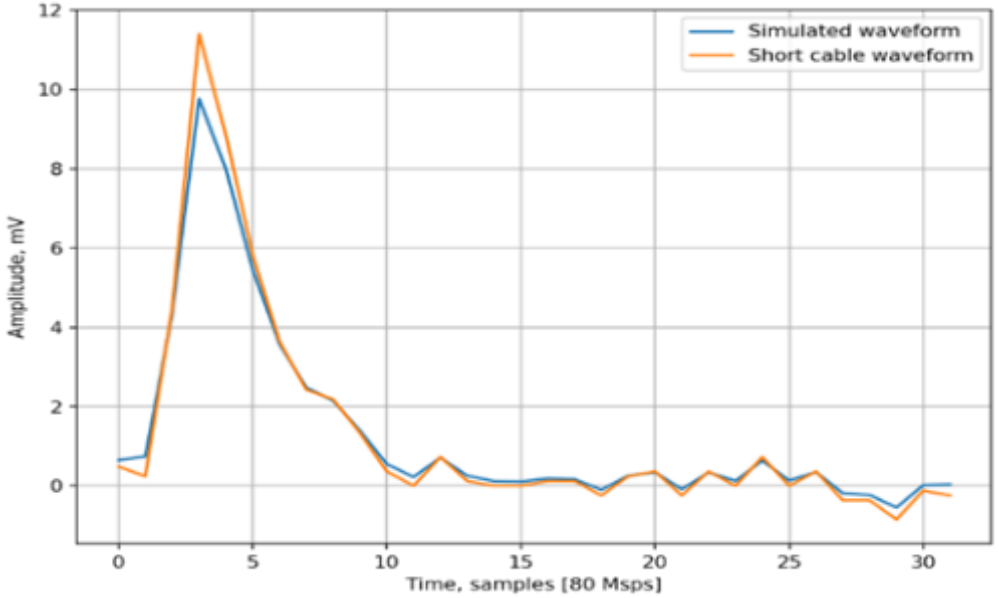
Signal cable verification



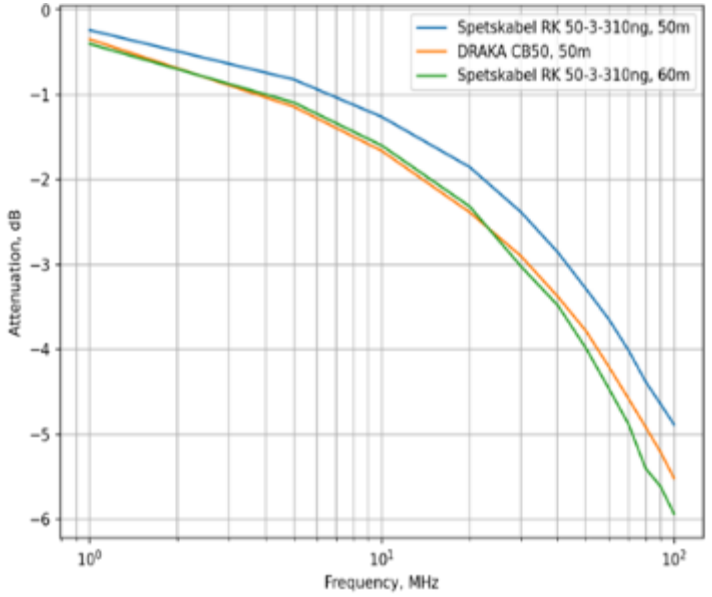
MPPC signals propagation via 50m cable



- Distance between radiation-hard “Detector side” and radiation-sensitive “Readout rack” is up to 55m
- 10 channel X 46 modules X 50m = 23 km signal cable
- РК50-3-310нг(С)-HF cables and DRAKA CB50 cables were tested
- Both cable show acceptable attenuation and skew, transmission of the signals without amplifiers is proven to be possible
- For 60 m cable attenuation is 1.5
- 60m cables used during beam tests at mCBM 2021

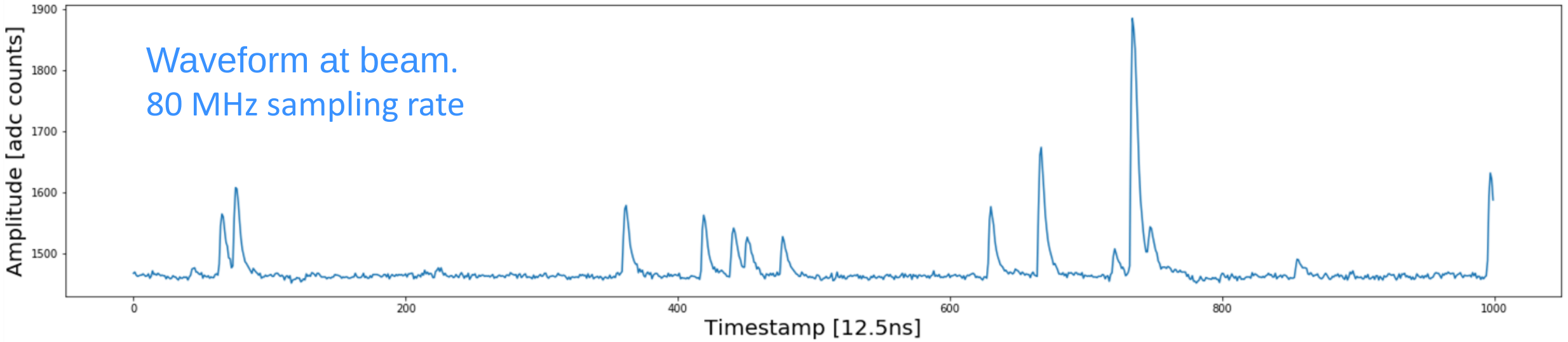


MPPC pulse waveform with cable’s frequency applied (estimation)

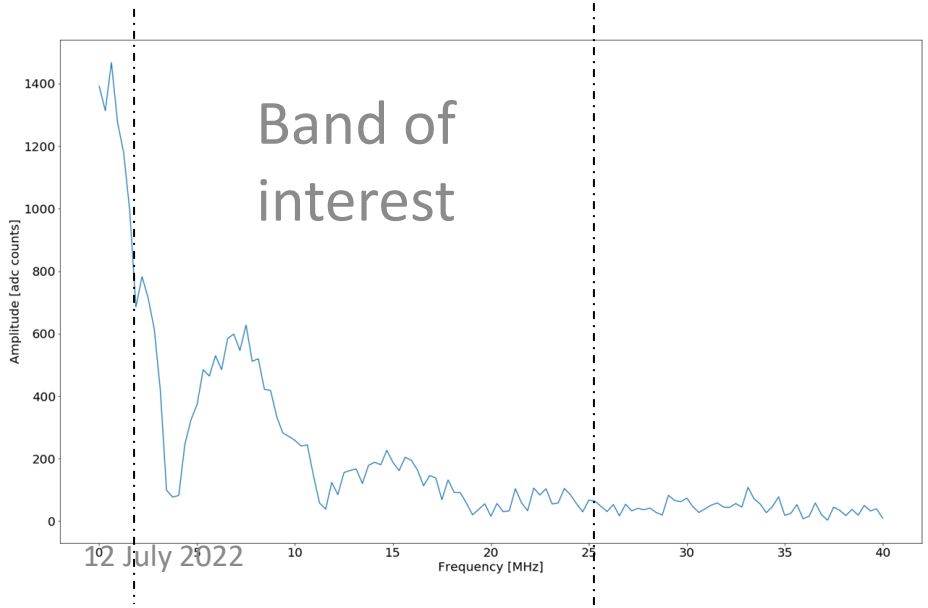


Cable frequency response

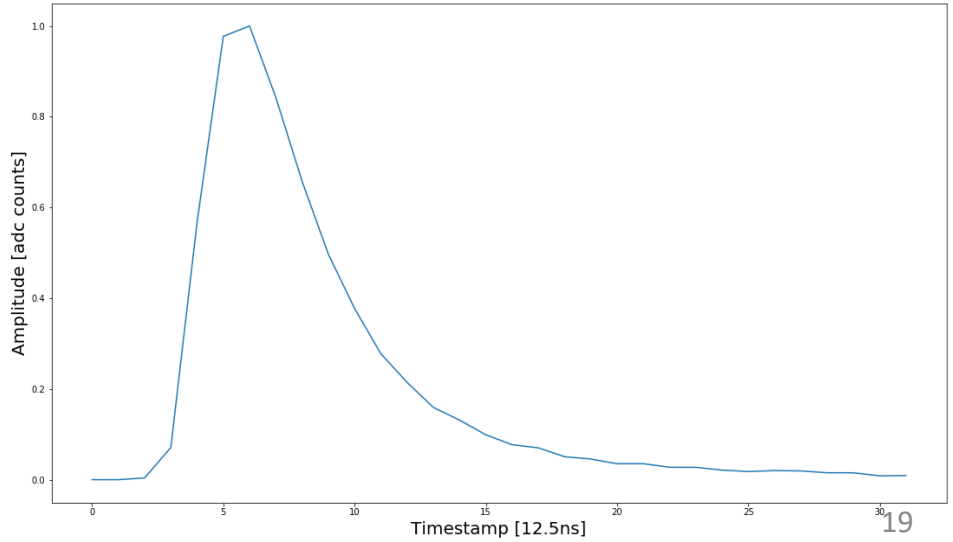
FIR filter design: Frequency Band Selection



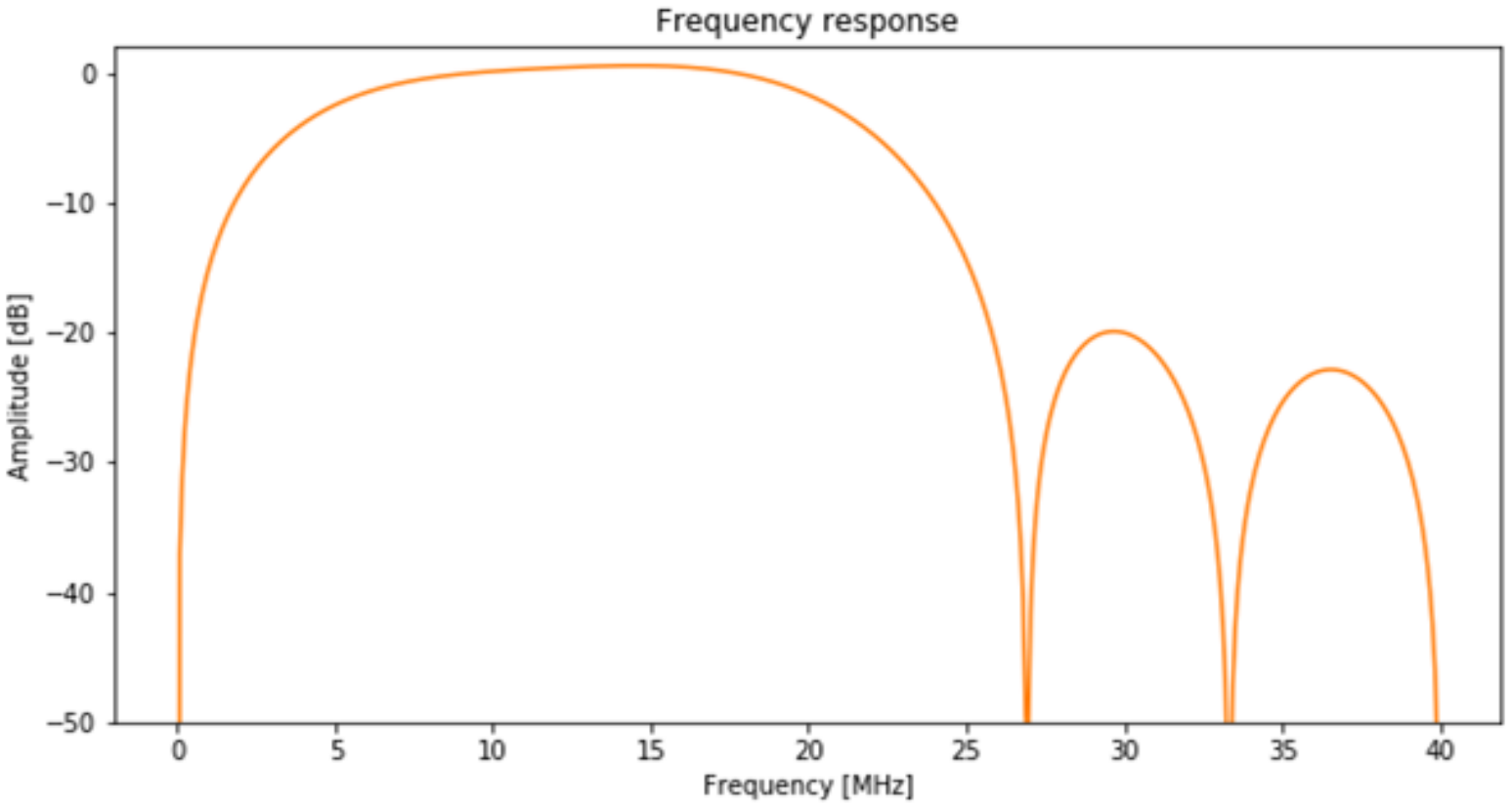
Spectrum of the detector signal



Typical signal waveform



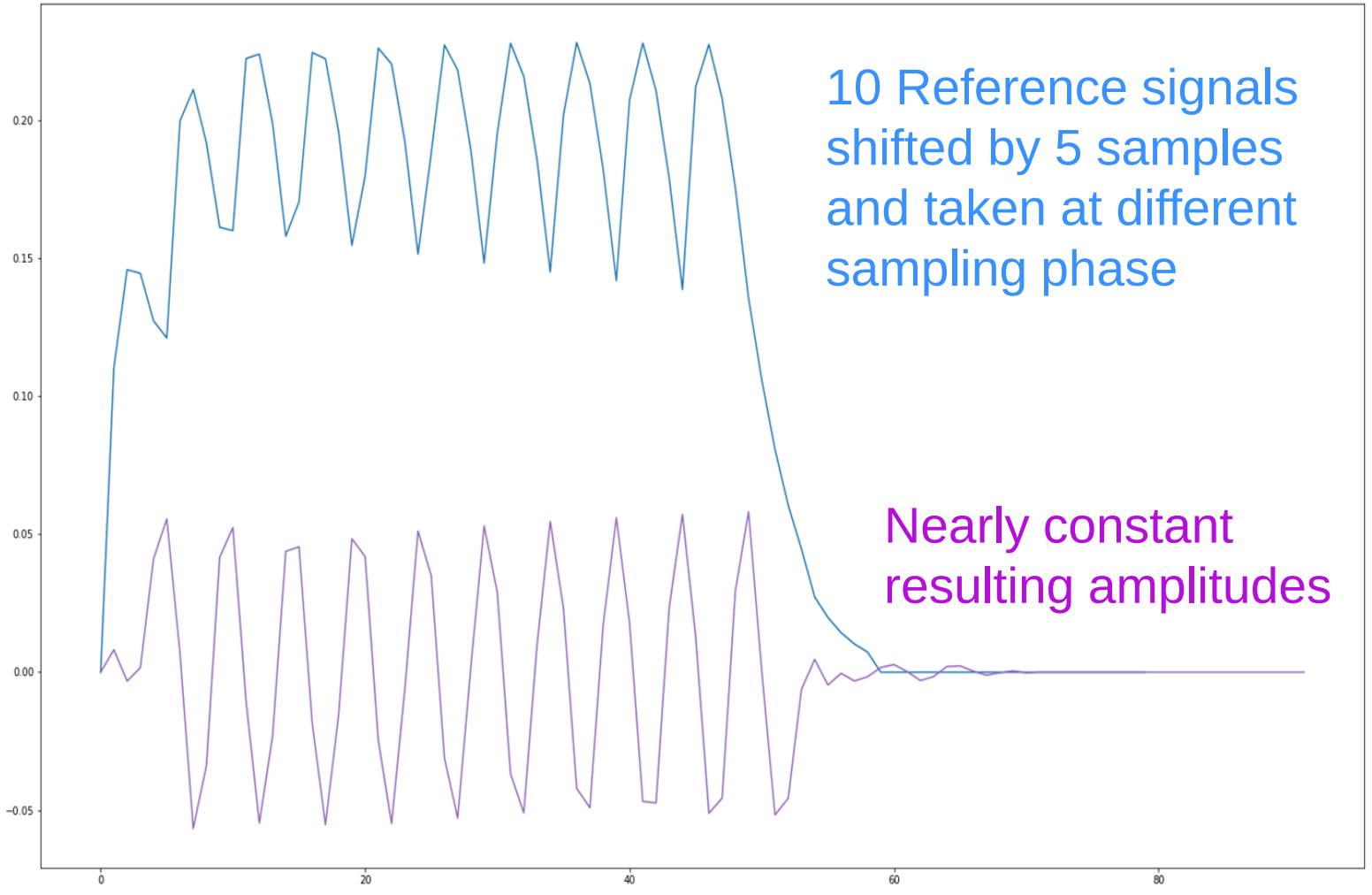
FIR filter design: Realization



Amplitude vs. frequency characteristic of the filter

- 11 multiplications
- low frequency drift cutoff
- high frequency noise rejection

FIR filter design: Resolving pile-ups

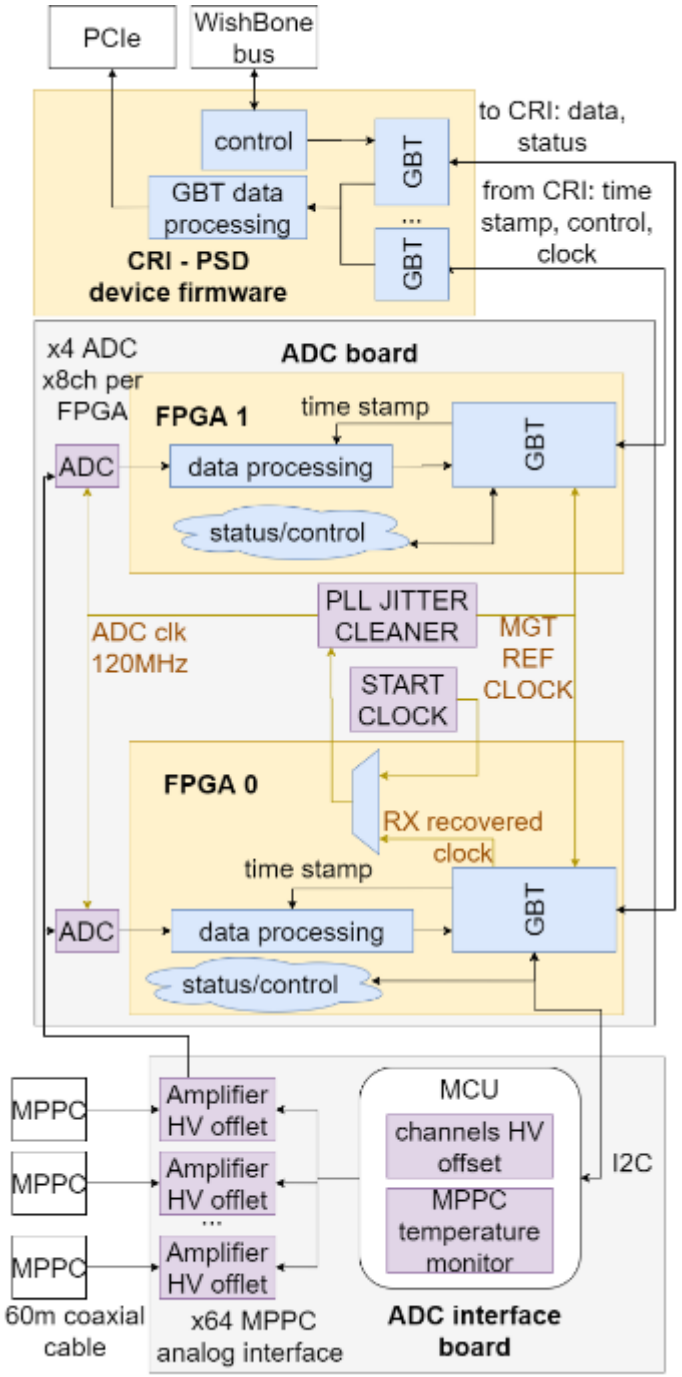


Testing FIR filter on pile-ups:

1. Take analytic description of Ethalon signal
2. Produce 10 signals with different sampling phase
3. Shift each by X sample
4. Investigate the limit case X

PSD full readout chain was tested at beam tests with common mCBM DAQ in June 2021

- ✓ FEE + 60m signal cable + ADC boards assembly
- ✓ GBT connection stability
- ✓ ADC signal digitizer firmware
- ✓ CRI data processing firmware
- ✓ ADC control + slow readout (python macro)
- ✓ Event time synchronization
- ❑ Issue was observed: ADC baseline drift during high rate because
  - ✓ Firmware exponential filter compensation was implemented for charge correction
  - ❑ Solution 2: Working on signal FIR processing FPGA with self-channel triggering without threshold-crossing procedure
- ❑ One FPGA on board was used during the tests
- ❑ 80 MHz ADC clock used, 120 MHz clock is not ready

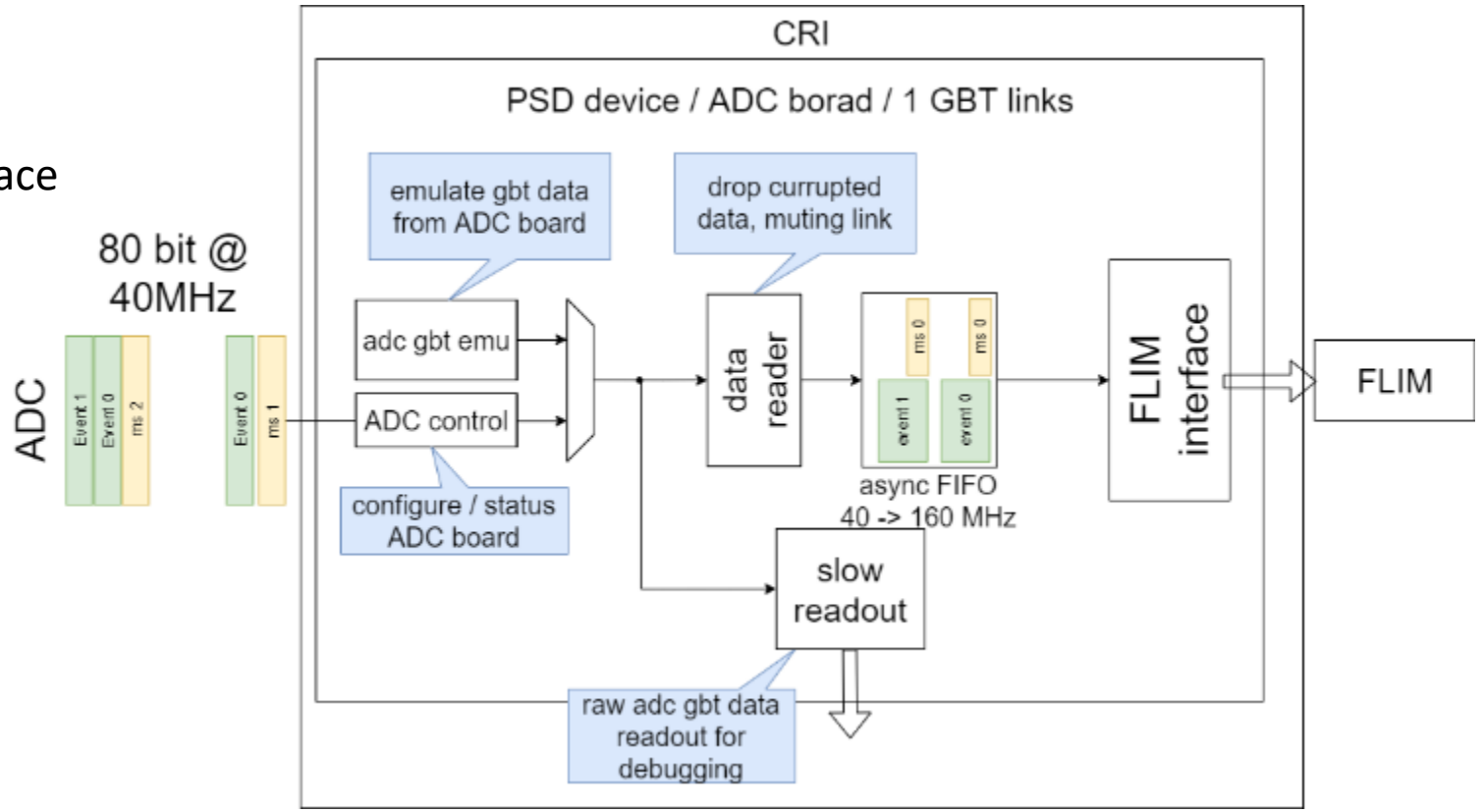


PSD-CRI firmware specific unit revision

- Data sorter will be excluded as excess element
- Single GBT link per FLIM interface
- Max FLIM interface load 64+16 bit @40MHz through async FIFO
- 8 ADC boards, 16 GBT links in total for PSD
- 8 FLIM interfaced / 8 GBT links per SLR
- PSD GBT spare solution is use wide bus mode:
  - 120bit @40MHz = 4,8Gb/s per FLIM interface
  - 38,4 Gb/s per SLR
  - 76,8 Gb/s per CRI

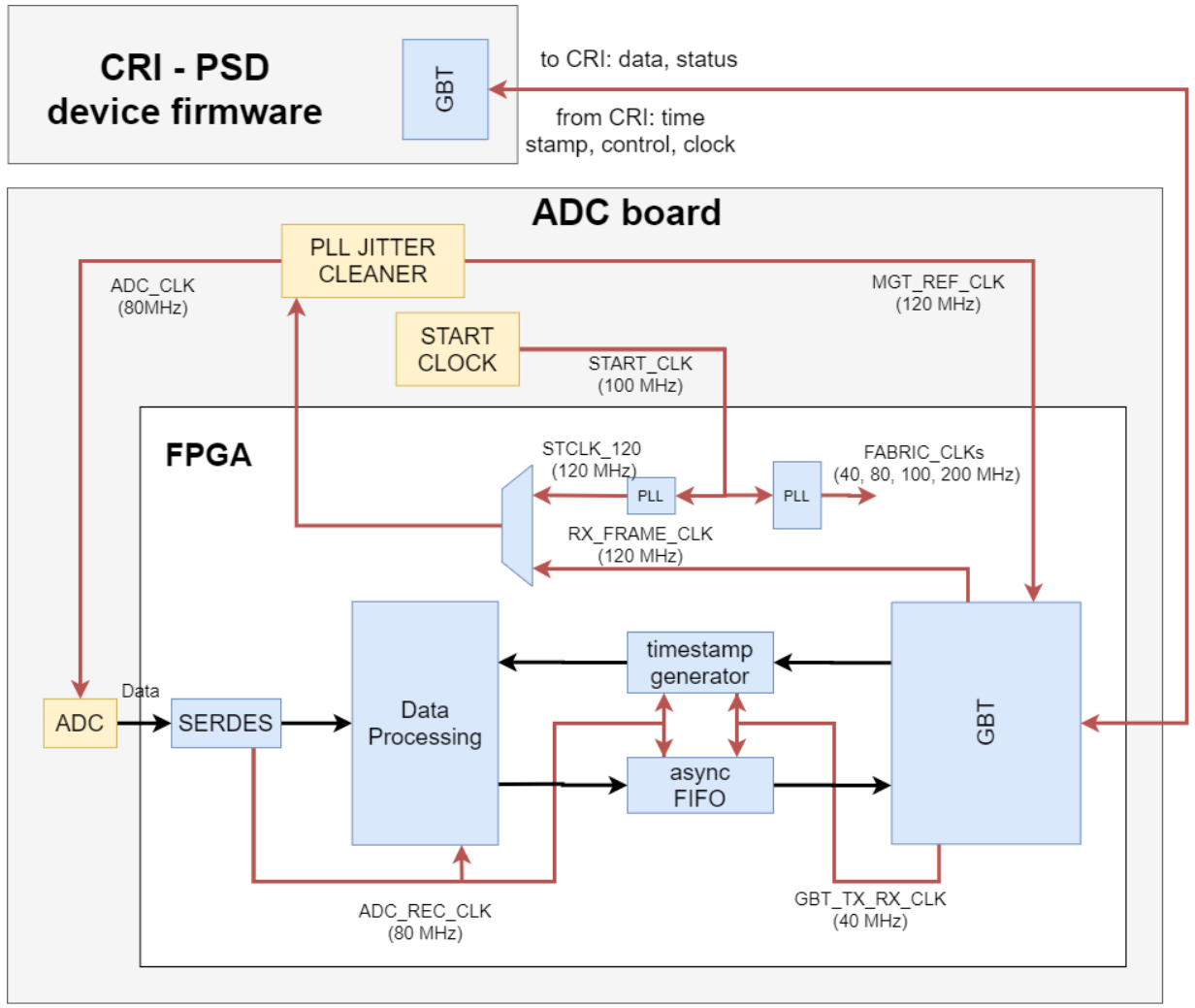
- No start/stop is required (always ready)
- No huge buffering data
- Input throughput = output throughput

FLIM throughput:
PCIe 6-7GB/s
50 Gb/s per SLR
100 Gb/s per CRI



Разработанная логическая структура ПЛИС платы ADC

Схема тактовых сигналов логической структуры ПЛИС платы ADC



Логическая структура ПЛИС для платы ADC обеспечивает:

- Формирование событий в бестриггерном режиме при загрузке детектора до 1 МГц
- Временную синхронизацию с остальными детекторами CBM
- Передачу данных по протоколу GBT
- Управление электроникой системы сбора данных PSD

Функциональные возможности прошивки ПЛИС включают:

- Регистрация сигналов по превышению порога независимо в каждом канале
- Обработка сигналов с применением фильтра FIR (Finite Impulse Response) для разделения наложений сигналов и определения событий независимо от базовой линии (в разработке)

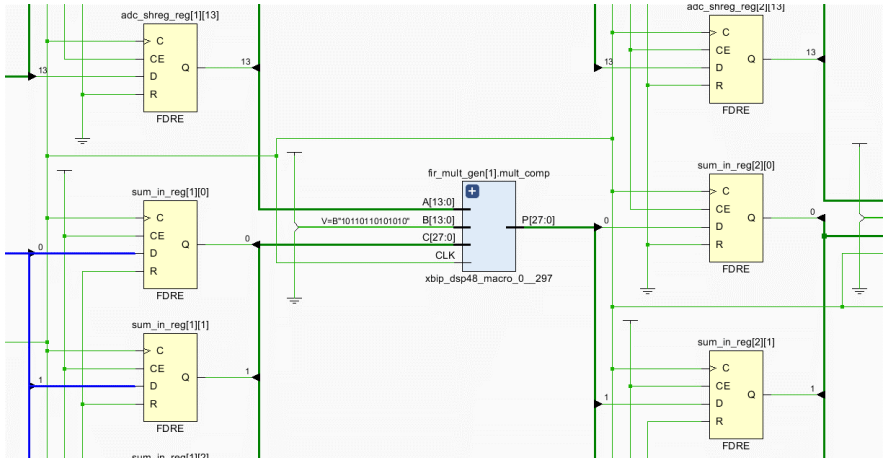
- Внутренний триггер формируемый от срабатывания выбранных каналов или с фиксированной частотой
- Отправка формы сигнала для отладки
- Контроль набора данных: нулевой уровень канала, уровень шума базовой линии, скорость набора данных, информирование об ошибках

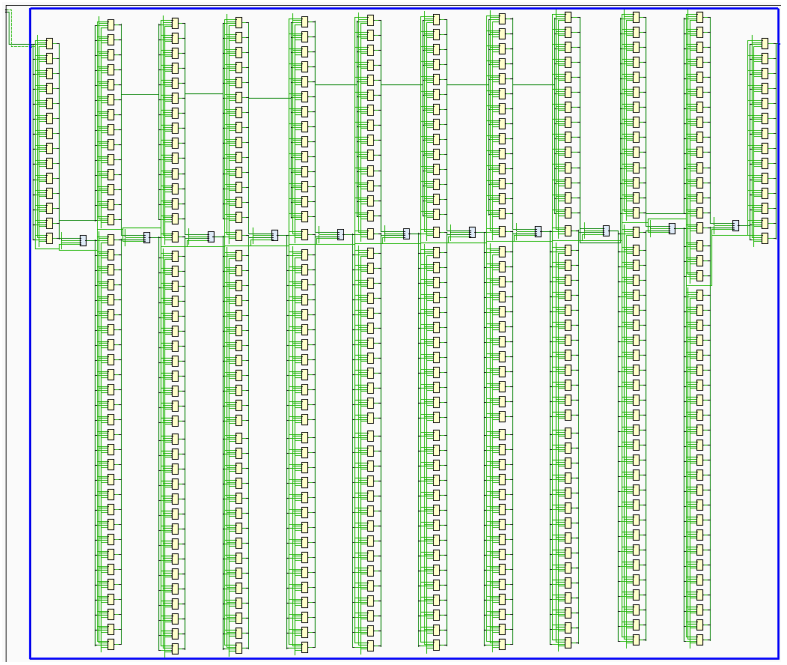
Разработанная логическая структура ПЛИС была протестирована на стенде в ИЯИ и на тестовых пучках установки mCBM

Emulation of signal FIR filter placement in FPGA KC7

11 DSP modules was implemented in ADC firmware design to check FPGA resources availability for FIR signal processing

- A(i)*c1+A(i-1)*c2+...+A(i-10)*c11
- 11 x DSP: A(14 bit) * B (14bit) + C(28 bit) = P(29bit) @80MHz
- DSPi: adc(i) * const(i) + dsp_out(i-1)(27 downto 0)





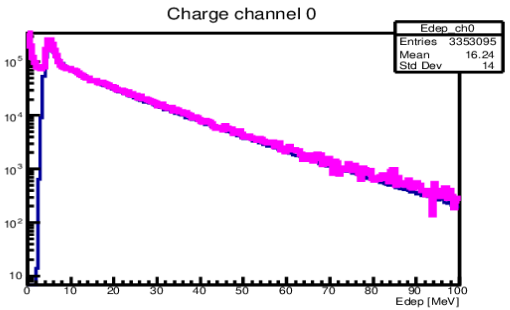
Site Type	Used	Fixed	Available	Util%
Slice LUTs*	57343	0	101400	56.55
LUT as Logic	55254	0	101400	54.49
LUT as Memory	2089	0	35000	5.97
LUT as Distributed RAM	34	0		
LUT as Shift Register	2055	0		
Slice Registers	146164	0	202800	72.07
Register as Flip Flop	146164	0	202800	72.07
Register as Latch	0	0	202800	0.00
F7 Muxes	995	0	50700	1.96
F8 Muxes	6	0	25350	0.02

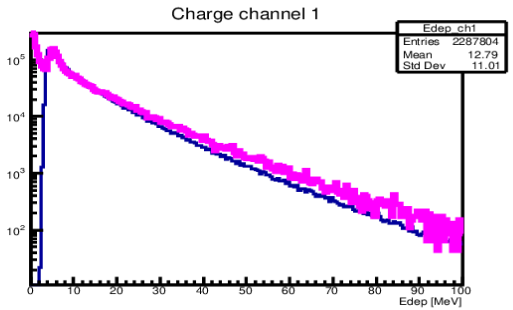
Site Type	Used	Fixed	Available	Util%
DSPs	352	0	600	58.67
DSP48E1 only	352			

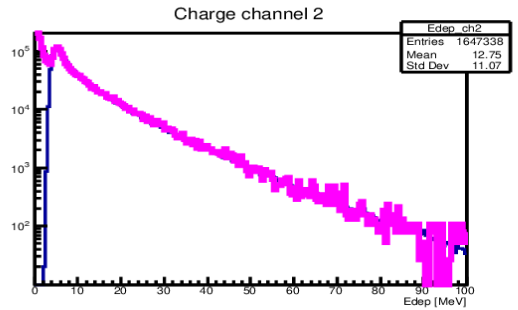
ADC FPGA utilization

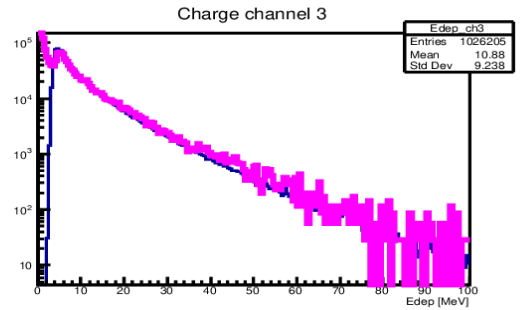
beam tests mCBM@2021 design + FIR emulation

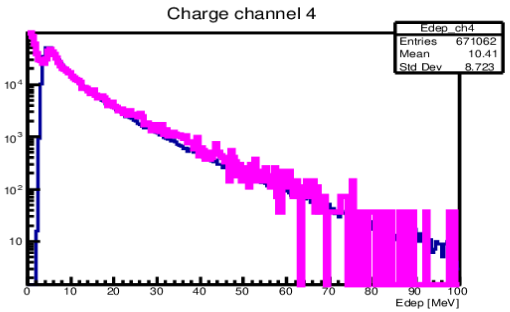
Спектры энерговыделения в секциях модуля mPSD

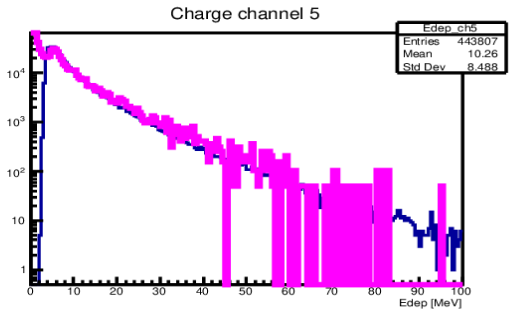


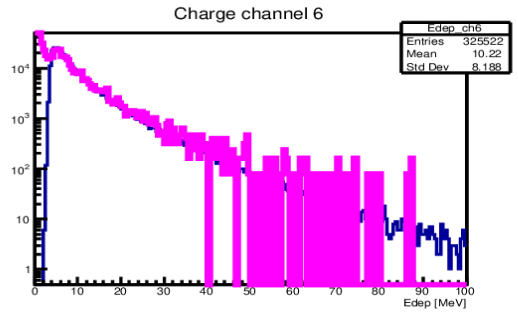


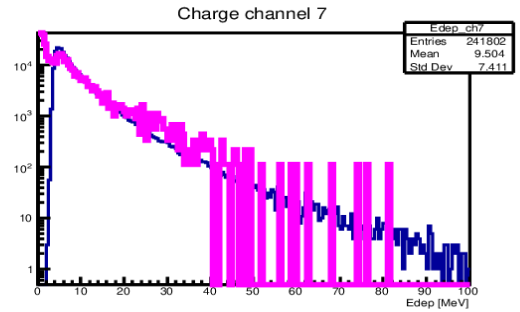


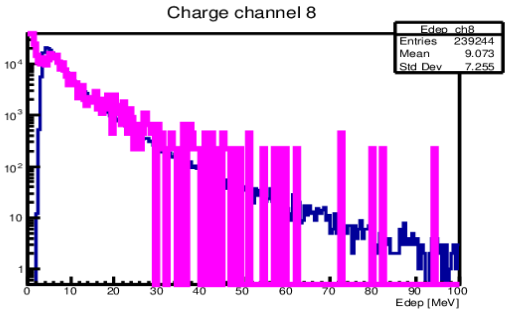


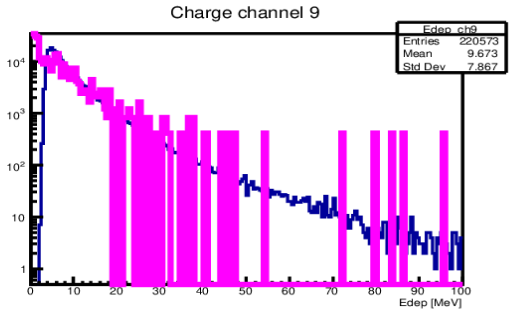












Run 1588 O+Ni 2.0AGeV

0.7MHz interaction rate

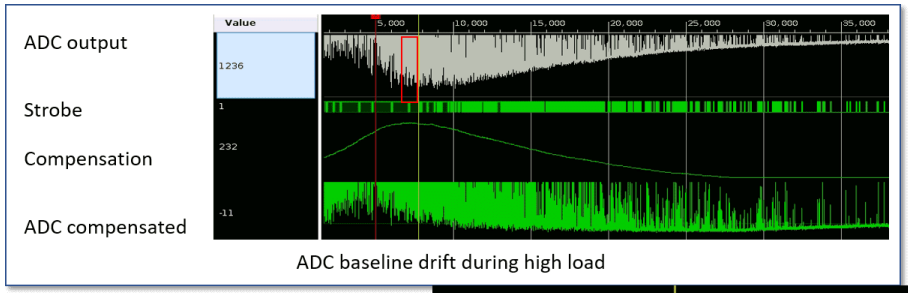
Taken 15.07.2021

Experiment & Simulation

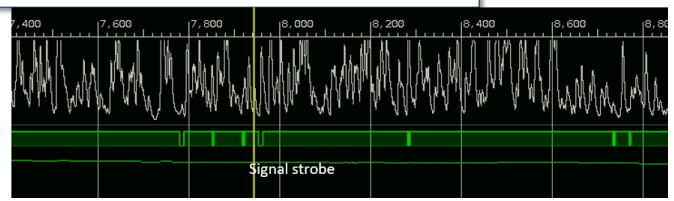
ADC baseline drift during high rate

ADC baseline drift during high rate because of capacitance in FEE input filter

- The firmware exponential filter compensation was prepared for beam tests.
- Correction allowed to measure signal charge with base line drift during the beam test.
- Because of tuned threshold ~ 0.8 MIP (1,4mV) compensation accuracy was not enough to avoid continuous triggering during base line drift.
- Data processing will be based on FIR filter (Finite Impulse Response) F(i) = A(i)*c1+A(i-1)*c2+...+A(i-10)*c11

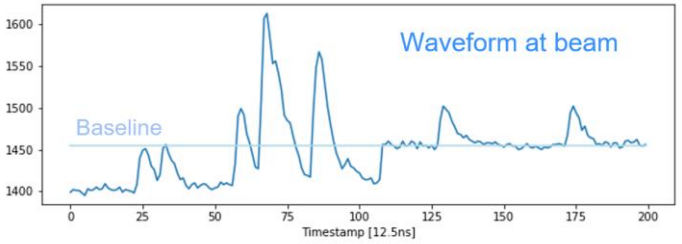


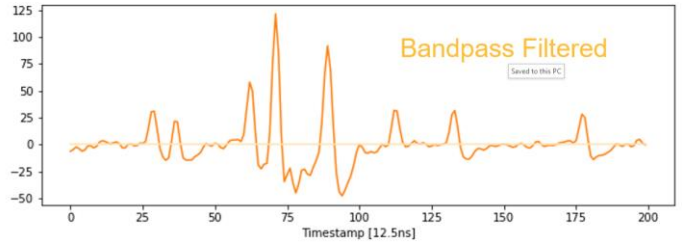
ADC baseline drift during high load

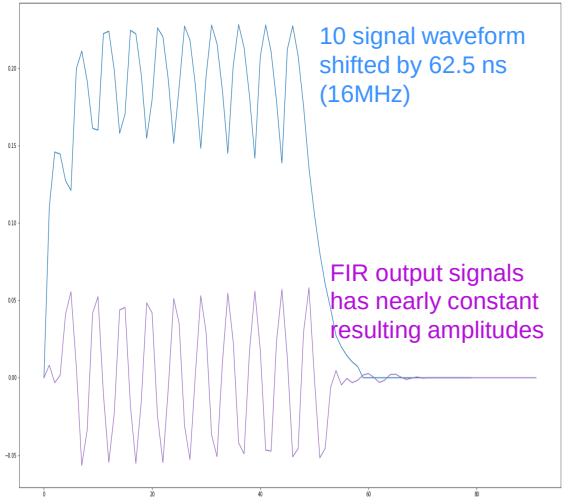


Continuously signals triggering

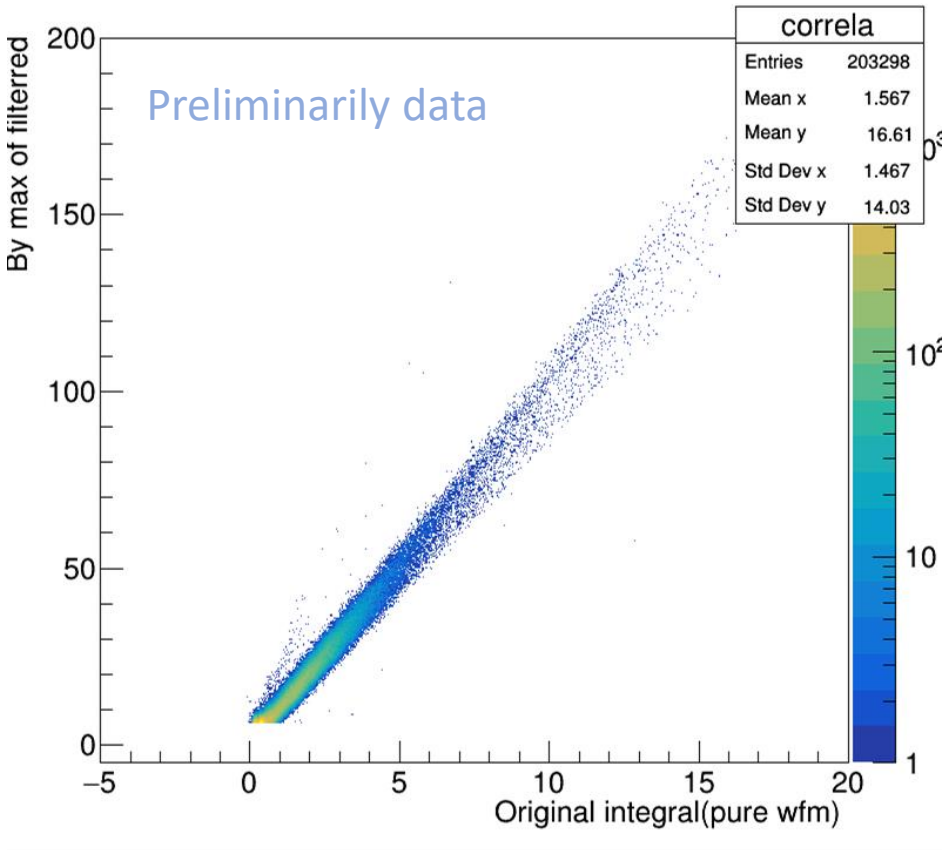
- FIR filter will allow:
  - Measure charge of overlapped signals. 10% pile-up at 1 MHz event rate
  - Event triggering without of baseline
  - Reduce the hit data size up to 20bits (4 MHz readout rate)
  - FIR filter was simulated in python with data from mCBM testbeam

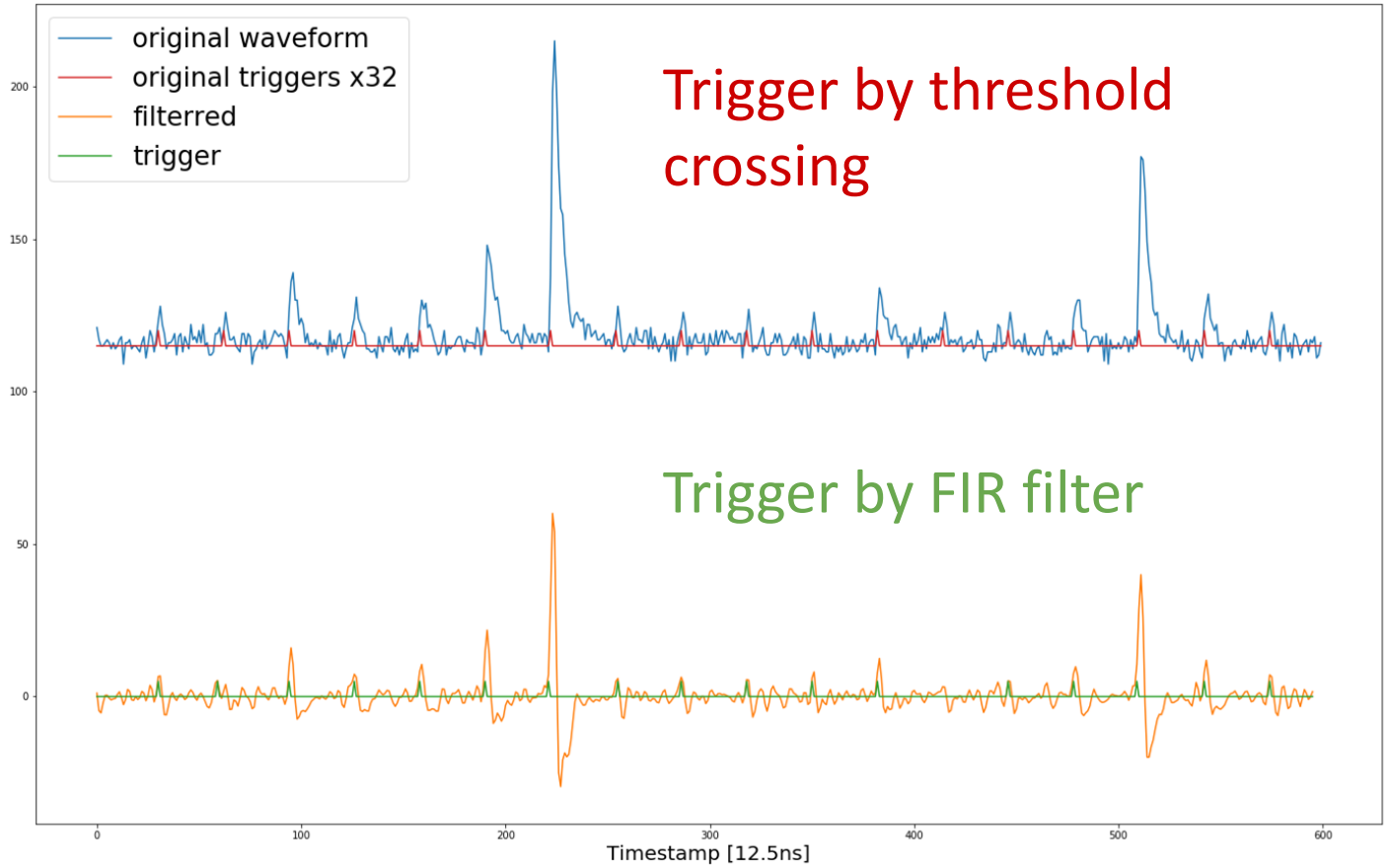






Hits finding with FIR filter

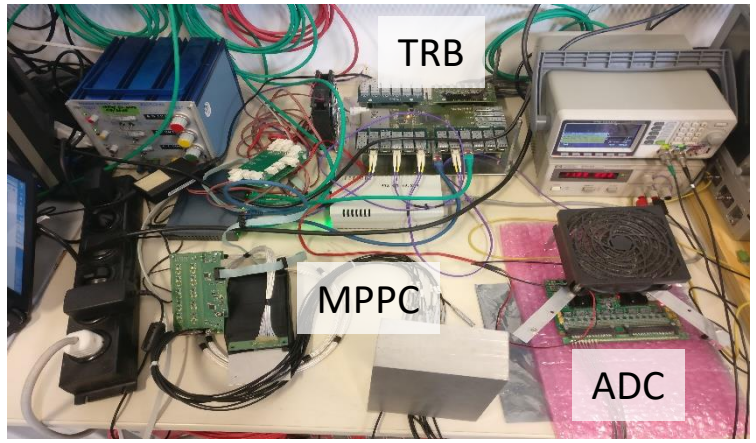




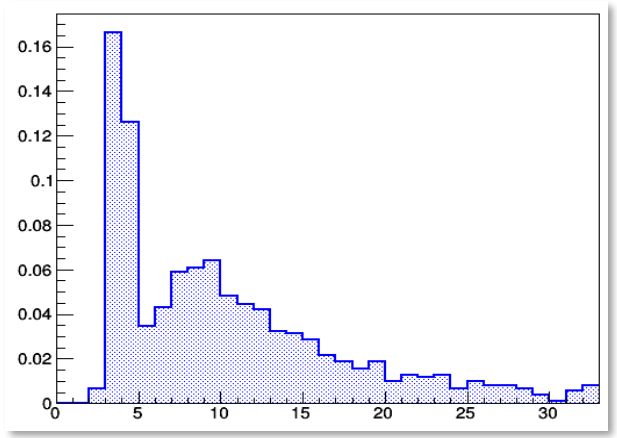
- Stable 1 MIP signal triggering without data losses
- FIR filter output has linear correlation with origin signal charge

Тестирование платы ADC по «оцифровке» сигналов фотодетекторов PSD

- Перед началом работ по интеграции платы ADC в систему сбора данных CBM ее необходимо было протестировать с фотодетекторами MPPC
- Был собран стенд по набору данных платой ADC системой сбора дынных калориметра EMC@PANDA на основе модуля TRB. Три ПЛИС платы TRB использовались в качестве «концентратора данных», «UDP конвертера» и «управляющей системы»
- Использовалась плата с MPPC для калориметра NA61
- Плата ADC была предоставлена в институте KVI-KART (г. Гронинген, Нидерланды) и имела парное усиление на канал x1 и x10 с входным фильтром.
- **Результаты теста показали стабильную работу платы и возможность оцифровки сигнала на уровне 1 MIP с фотодетекторов PSD**

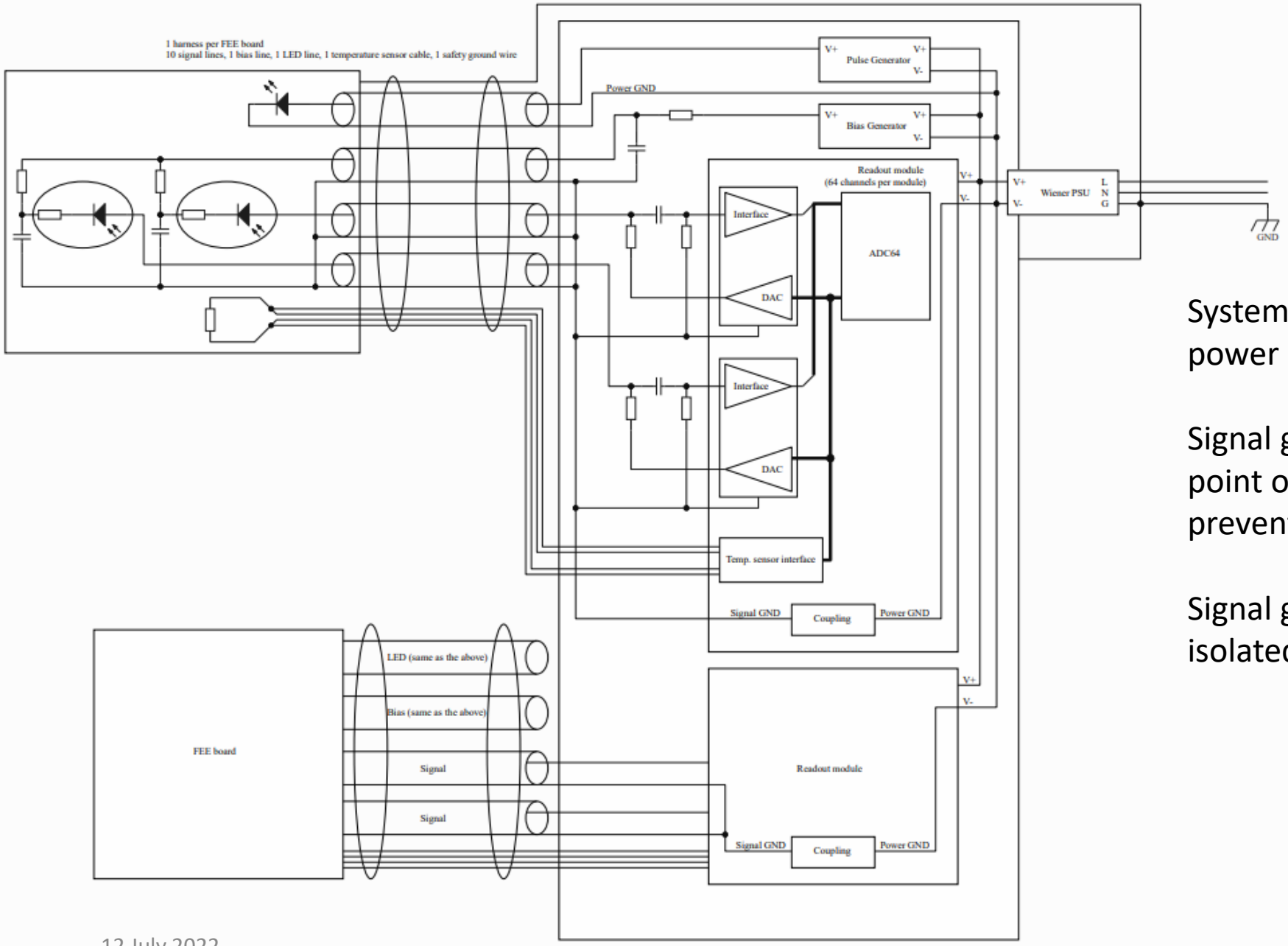


Фотография стенда оцифровки сигналов платой ADC прототипом системы сбора данных ECAL@PANDA



Амплитудный спектр от космических мюонов, мВ

Grounding schematic



System has independent signal and power grounds.

Signal grounds has coupling in one point on the readout module, which prevents the ground loop currents.

Signal ground on the FEE board is isolated from metal structures.